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# Partitioning and Floorplanning

# Partitioning

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- Decomposition of complex systems into smaller Subsystem
- Each subsystem can be designed independently
- Decomposition scheme has to minimize the interconnection between the systems
- Decomposition is carried out hierarchically until each subsystem is of manageable size.

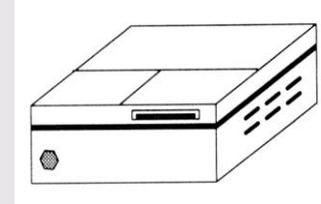
# Levels of Partitioning



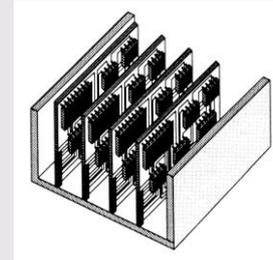
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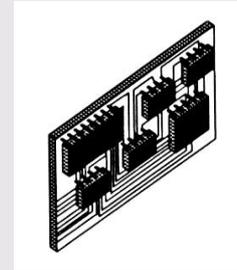
System Level Partitioning



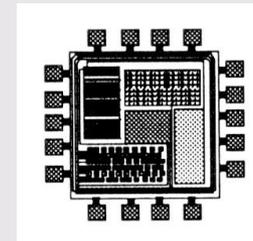
System



PCBs



Chips



Subcircuits  
/ Blocks

Board Level Partitioning

Chip Level Partitioning



# Circuit Representation

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**Netlist:**

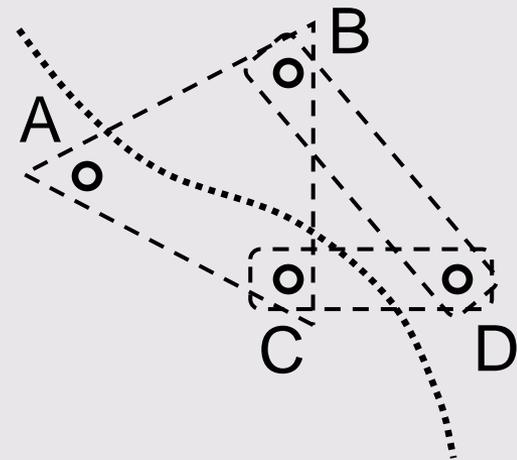
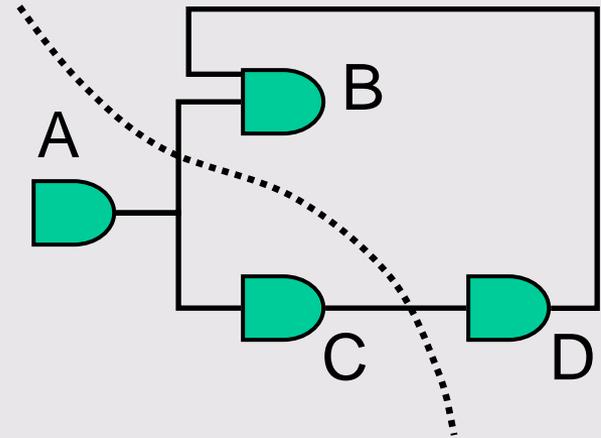
Gates: A, B, C, D

Nets: {A,B,C}, {B,D}, {C,D}

Hypergraph:

Vertices: A, B, C, D

Hyperedges: {A,B,C}, {B,D}, {C,D}



# *Partitioning Rule*

  
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Interconnection between the Partition is minimized.

Delay due to partitioning is minimized.

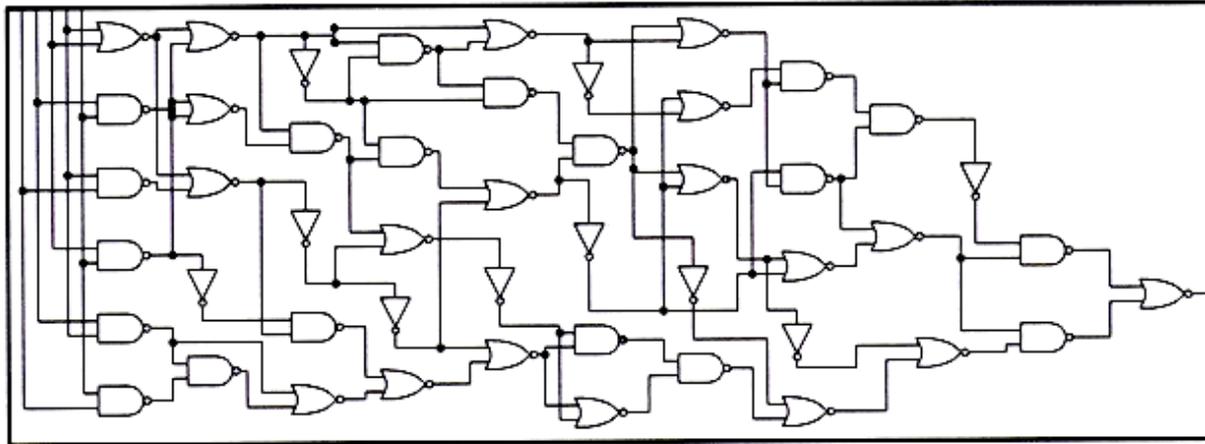
Number of terminals less than predetermined maximum value.

The area of each partition remains within specific bounds.

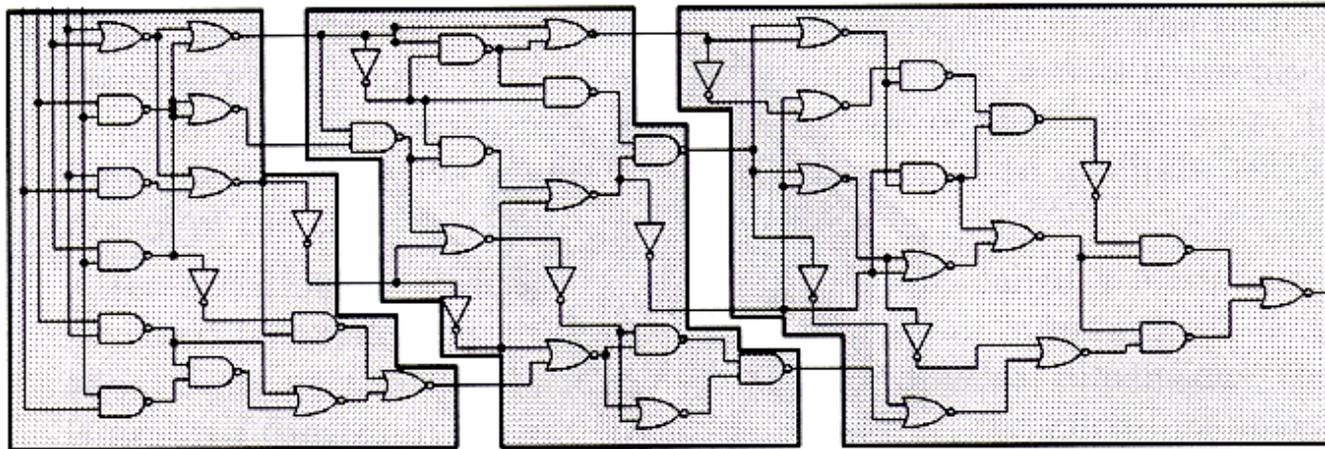
# Partitioning of a Circuit



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(a)



(b)

# *What is Floorplanning ?*

  
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Floorplanning nothing but a plan a house Floorplanning.

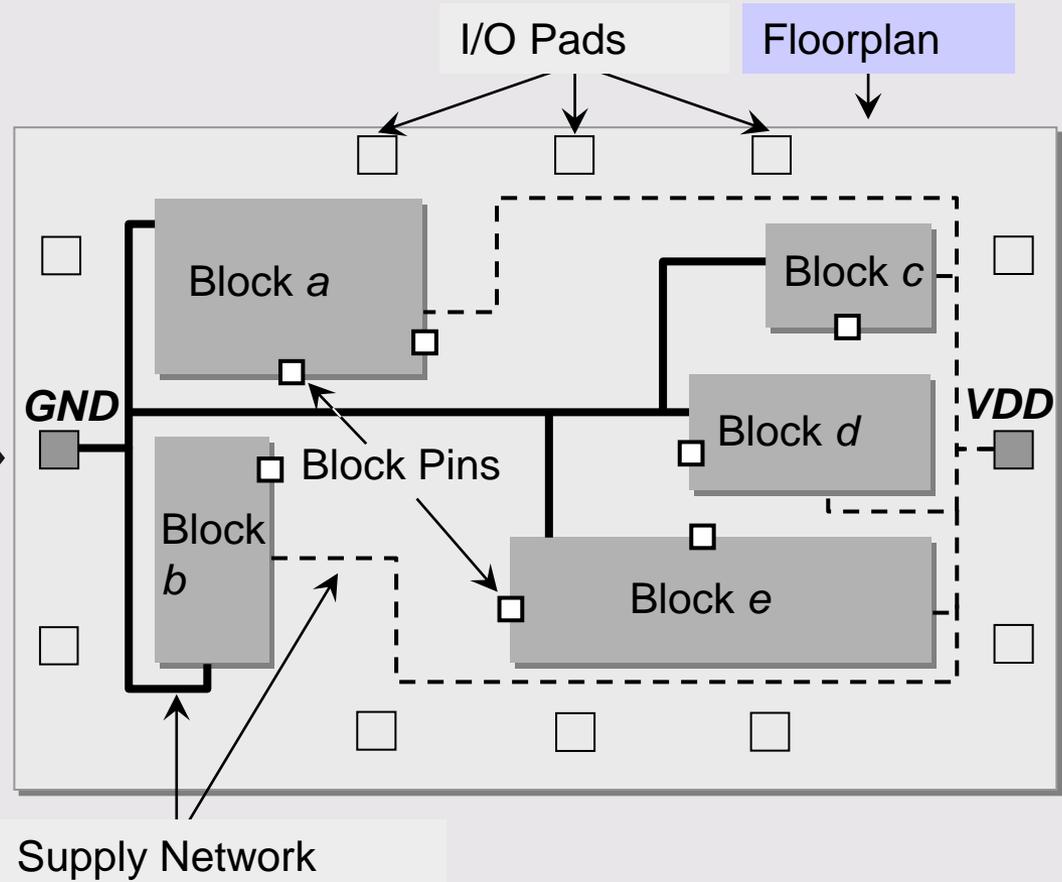
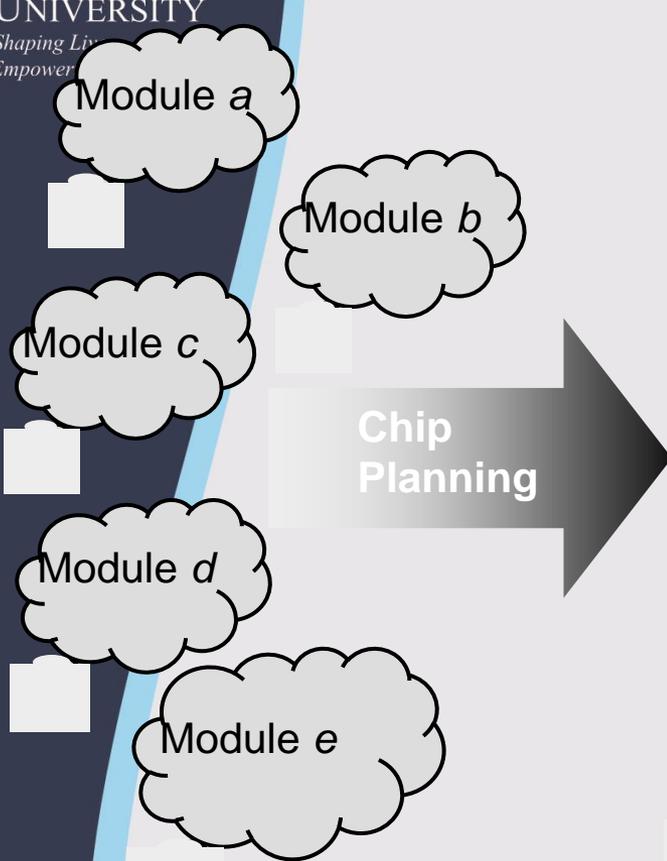
Find approximate locations of a set of modules that need to placed on layout surface.

Available region typically considered rectangular, modules are also typically rectangular In shape but there can be exceptions(e.g-Lshape)

# Typical Floorplan

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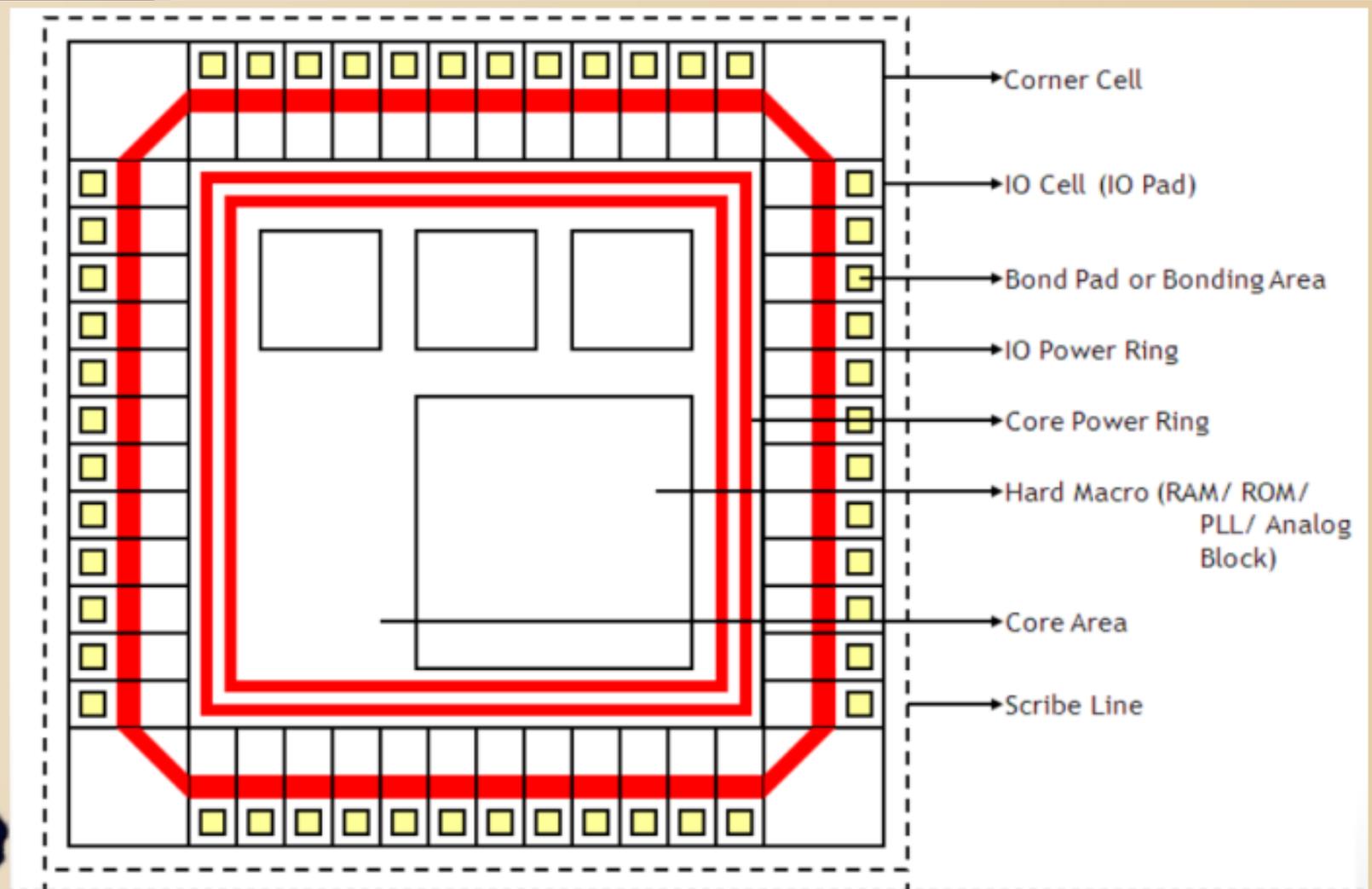


# Floor plan Terminology

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# *Floorplan Goals*

  
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- Partition the design into functional blocks
- Arrange the blocks on a chip
- Place the Macros
- Decide the location of the I/O pads
- Decide the location and number of the power pads
- Decide the type of power distribution

# *Floor Plan Inputs*

  
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Synthesis Netlist

Physical Libraries

Logic Libraries

Timing constraints

Power requirement

Floor planning control parameters

# *Synthesis Netlist*

  
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A netlist is a description of the connectivity . In its simplest form, a netlist consists of a list of the electronic components in a circuit and a list of the nodes they are connected to.

It can be in the form of Verilog or VHDL.

This netlist is produced during logical, synthesis, which takes place prior to the physical design stage.

# *Physical Library*

  
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**Physical/Reference libraries** contains physical information of standard, macro and pad cells, which is necessary for placement and routing.

These libraries define placement file like height of placement rows, minimum width resolution, preferred routing direction pitch of routing tracks.

# *Logic Libraries*

  
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This library file which provides timing and functionality information on each and every standard cells used in the design. It also provides timing information such as IP,ROM, RAM etc.

# *Timing Constraints*

  
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SDC constraints. Clock constraints - max skew, max and min insertion delay, no. of clock domains, clock start points (whether port level or internally generated)

# *Floor Planning Problem*

  
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The floorplanning problem is to plan the positions and shapes of the modules at the beginning of the design cycle to **optimize the performance of the circuits:**

- chip area
- total wirelength
- delay of critical paths
- routability
- In floorplanning several alternatives for each block are considered

# *Floorplan Challenges*

  
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## Die Area

- Congestion
- Timing
- Power Network Design
- Electro-Migration
- IR Drop