

CENTURION UNIVERSITY OF TECHNOLOGY & MANAGEMENT

SCHOOL OF ENGINEERING & TECHNOLOGY

VLSI DESIGN

Assignment-3

Date of submission: Before External Exam

SEM: CBCS

Short Questions:-

1. Define set-up time and propagation Delay
2. Write VHDL syntax for entity and architecture.
3. How fan-out of a gate is specified?
4. Draw the layout of CMOS Inverter.
5. Define fan-in and Fan-out.
6. Write VHDL program for the Boolean expression: $Y = abc + a'b'c$
7. Expand VHDL and HDL?
8. What is a ring counter?
9. What is a decade – counter?
10. What are the applications of counters?
11. Draw the symbols for MOSFET- n & p channel.
12. What is a register?
13. What are the types of Register ?
14. What are the applications of Registers?
15. Write a program in dataflow model for the following:
 - o All the logic gates
 - o Half adder, Full adder
 - o 4:1 multiplexer

Long questions:-

1. Design a synchronous counter to produce the following binary sequence use JK flip-flops 0,9,1,8,2,8,3,6,4,5,0.....
Design a counter using JK FF which counts 1,2 ,3,8,3,5,12....
2. Draw a logic diagram of a 8-bit parallel in serial out shift register. Explain its working, why a CLKINH is provided?
3. Input data is 11001010. Draw the appropriate timing diagram showing load, inhibit, and serial shift.
4. Write short notes on
 - a. Programmable array logic
 - b. A CMOS inverter and its operation
 - c. Circuit implementation
5. Design and implement a mod-6 asynchronous counter using T flip-flops.
6. Design a combinational circuit using ROM .The circuit accepts 3bit number and generate an output binary equal to square of input number
7. Write the VHDL code for 8:1 Mux. Assume that the complement AND_4G, OR_8G and NOT_1G are already designed which will represent 4 input AND,8 input OR and NOT gate respectively.
8. Draw the CMOS circuit for NOT gate and give the neat sketch of layout.
9. Describe in brief the construction, circuit diagrams and operations of MOS and CMOS logic circuits.

10. Draw the logic diagram of the digital circuit specified by following HDL

```
module circct( A,B,C,D,F);  
    input A,B,C,D;  
    output F;  
    wire w,x,y,z,a,d;  
    and (x, B,C,d );  
    and (Y,a,C);  
    and (w,z,B);  
    or (z,y,A);  
    or( F,x,w);
```

```
not (a,A);  
not (d,D);  
endmodule
```

11. Implement CMOS inverter, NAND and NOR circuits. -BPUT: 2008(A)

12. Write HDL Program for the following circuits

