

## QUESTION BANK

1. Convert the number  $(294.675)_{10}$  to hexadecimal.
2. Solve  $(11100101)_2 - (10100110)_2$  following 2's complement method.
3. Simplify  $AB + A'C + ABC + A'BC$  to a minimum no of literals.
4. Determine the base of the following operation;  $24 + 17 = 40$
5. What is "prime implicant" in K-Map? When will we tell them essential?
6. Express the following in its canonical form.  $AB + A'C + AB'C$ .
7. What is race around problem in JK flip-flop? How can it be removed?
8. Draw the gate level diagram of T flip flop using NAND gates only.
9. Differentiate between synchronous and ripple counter.
10. What is Johnson Counter?
11. What is FPGA?
12. Carry out the following operation  $(110010 - 100111)$  using 1's complement notation.
13. Draw a multi-level NAND gate circuit to implement  $(AB' + CD')(E + BC)(A + B)$
14. What do you mean by sequential logic circuit? Distinguish between synchronous and asynchronous logic circuit.
15. What is ring counter?
16. Design a 3 to 8 line decoder using two 2 to 4 line decoder with enable input.
17. Draw the diagram of a JK latch using Only NAND gate?
18. What is Race-around condition? How this problem will be resolved?
19. Differentiate between synchronous and asynchronous circuit?
20. With suitable example distinguish between PAL and PLA?
21. Write the excitation table for JK F/F.
22. Why both "S" and "R" inputs and a SR latch should never be "1" simultaneously.
23. What will happen if the frequency of the clock signal connected to a F/F is increased to a very high value or decrease to a very low value.
24. Distinguish the functions of decoder, Encoder and multiplexer
25. What is called as 3-state gate? What is its importance in combinational circuit?
26. Implement the full adder circuit using decoder.
27. What is the difference between latch and F/F.
28. What do you mean by sequential logic circuit? Distinguish between synchronous and asynchronous logic circuit.

29. What is called as characteristic equation? Write the characteristic equation for SR and D F/Fs.
30. What is excitation table? Write the excitation table for all F/Fs.
31. Design a BCD to decimal decoder
32. Design a 3-bit GRAY code to Binary converter
33. Design a 3-bit Binary to GRAY code converter
34. Design a circuit for the subtraction of two unsigned binary numbers .explain its operation
35. Realize a full adder using 4:1 MUX.
36. Binary number system is used in digital electronics circuits. Why octal, decimal or hexadecimal number systems are not used in circuit levels?
37. What will be the correct answer during subtraction of unsigned numbers using 1's complement method for the following? Mention whether the answer is a positive number or a negative number.
- End carry occurs.
38. End carry does not occur.
39. What is “prime implicant”? When it is said to be essential?
40. Convert the following function to “product of sums”.
- $$F = A'B'C + AB'C' + AB'C + ABC' + ABC$$
- Are “NOR-OR” and “OR-NAND” functions equivalent? Justify.
41. Obtain the truth table of the following functions and express in sum-of-min terms and product-of-max terms.
- $$(XY + Z) (Y+XZ)$$
42. Find the complement of  $F = X + YZ$ ; then find the values of  $F$ ,  $F'$  AND  $F+F'$ .
43. carry out the following addition:
- a. (+13, -11) using 1's complement notation.
  - b. (-15, +9) using 2's complement notation.
44. Add the following using signed magnitude system.
- |          |          |
|----------|----------|
| +8 & +14 | +8 & -14 |
| -8 & +14 | -8 & +14 |
45. What is the range of unsigned decimal values that can be represented by 8 bits?
46. How many bits are required to represent decimal values ranging from 75 to -75?

47. Apply Demorgan's theorem to prove that

$$AB + CD + EF = (A + B)(C + D)(E + F)$$

48. Give the truth-table of a function  $f(x,y)$  where  $f(x,y) = 1$  when  $x = y$ .

49. Implement with Two-level NOR gate circuit  $F(w, x, y, z) = \Sigma(5, 6, 9, 10)$

50. Draw a multi level NAND gate circuit  $(AB' + CD')(E+BC)(A+B)$

## LONG QUESTION

1. Simplify the function  $f(ABCD) = \Sigma_m(0,1,2,3,8,9,10)$  and  $d(ABCD) = \Sigma_m(6,11)$  using k map and implement by using only NAND and only NOR
2. Express the following in Canonical SOP and POS,  $Y = A'B + AC$ .
3. Write the HDL code for a Half Adder.

4. Design a 4 to 2 line priority encoder with LSB priority.

5. Implement the function  $f(ABCD) = \Sigma_m(1,3,5,6,10,11,15)$  using a 8:1 mux.

6. A sequential circuit has two JK flip flops A and B, one input X, and one output Y. The circuit is described by the following flip-flop equations  $J_A = X$ ,  $K_A = B'$ ,  $J_B = X+A$ ,  $K_B = AB$ ,  $Y = A + B$

Draw the State table and state diagram for the above.

7. Briefly explain the FPGA design process flow.

8. Briefly draw and explain the structure of a CLB.

9. Simplify the following function to a minimum number of literal using Boolean algebra

$$F = X\bar{Y}Z + \bar{X}\bar{Y}Z + \bar{W}XY + W\bar{X}Y + WXY$$

10. Using K-Map solve the following expression and implement using minimum number of i. NAND gates only, ii. NOR gate only

11. Write a Verilog code to implement Full subtractor in Structural Modeling.

12. Implement the following Boolean function using 8:1 multiplexer

$$F(A, B, C, D) = \Sigma 0,1,3,4,8,9,10,13,15$$

13. Design a combinational circuit that will implement  $2 \times 2$  multiplication?

14. Write a Verilog code to implement JK Flip Flop in Behavioral Modeling.

15. Design a synchronous counter to produce the following binary sequence use T- flip-flops  
0,9,1,8,2,8,3,6,4,5,0,.....

16. What is shift register? With suitable diagrams and timing waveforms explain the different type of shift registers?

17. Design a sequential circuit using D Flip Flop. The circuit accepts 3bit number and generate an output binary equal to 2's complement of the number?

18. Simplify the Boolean function using four variable maps:

- a.  $F(w, x, y, z) = \sum(1, 4, 5, 6, 12, 14, 15)$   
 b.  $F(a, b, c, d) = \sum(0, 1, 2, 4, 5, 7, 11, 15)$   
 c.  $F(w, x, y, z) = \sum(0, 2, 4, 5, 6, 7, 8, 10, 13, 15)$
- 19.** Use karnough map to reduce  $A + BC + CD$  to a minimum SOP form.
- 20.** Express the Boolean functions as a sum-of-min terms.  
 $F = A + B'C$  Now convert the sum-of-min terms to another canonical form
- 21.** Simplify the following Boolean function and draw a circuit to represent the function.  
 $F(W, X, Y, Z) = \sum(0, 1, 2, 4, 5, 6, 8, 9, 12, 13, 14)$
- 22.** Implement the following function.  
 •  $F = A(CD+B) + BC'$  using NAND gates.
- 23.**  $F = (A+B)(C+D)E$  using NOR gates.
- 24.** Using Karnough map convert the following standard POS expression into a minimum POS expression, a standard SOP expression and a minimum SOP expression:  
 $(A + B' + C' + D')(A' + B' + C + D)(A' + B' + C' + D)(A + B + C + D)$
- 25.** Use Karnough map to simplify the expression to a minimum SOP form:  
 $A'B'C' + A'BC' + AB'C' + ABC'$
- 26.** Simplify the following expression:  
 (A)  $AB + A(B + C) + B(B + C)$       (B)  $F = \sum m(1, 3, 5, 7)$   
 (C)  $F = \prod M(3, 5, 7)$       (D)  $F = (A + B + C + D) + ABCD$   
 (E). Show that  $AB + AB'C + BC = AC + BC'$
- 27.** Minimize the function  
 $F(W, X, Y, Z) = \sum(0, 1, 2, 3, 8, 9, 10, 11)$
- 28.** Find the complement of the following  
 (A)  $F = ABC + A'BC'$   
 (B) Convert the given expression into canonical SOP form:  
 (C)  $(A + B)(B + C')(C + A)$   
 (D) .Simplify the Boolean expression in (1) sum of product & (2) products of sum  
 (E)  $XZ + YZ + YZ + XY'$   
 (F)  $(A + B + D)(A + B + C')(A + B + D)(B + C + D)$
- 29.** Design a four bit magnitude comparator that compares two 4-bit numbers A and B to check if they are equal The circuit has output  $f=1$  if  $A=B$  and  $f=0$  if  $A \neq B$ .
- 30.** What is a priority encoder? Design a priority encoder having  $D_0$  as the highest priority and  $D_3$  as the lowest priority.
- 31.** Write Short Notes on

- a) Decoder
- b) Master Slave Design
- c) SISO register
- d) PLA
- e) Boolean Algebra
- f) Master Slave Flip Flop
- g) MSB Priority encoder
- h) PAL