

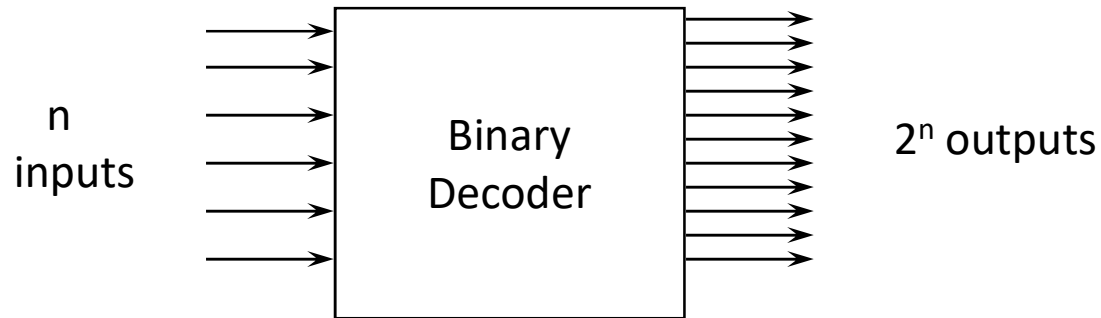
# Combinational Circuit(Decoder)

## Overview

- Binary decoders
  - Converts an n-bit code to a single active output
  - Can be developed using AND/OR gates
  - Can be used to implement logic circuits.
- Binary encoders
  - Converts one of  $2^n$  inputs to an n-bit output
  - Useful for compressing data
  - Can be developed using AND/OR gates
- Both encoders and decoders are extensively used in digital systems

## Binary Decoder

- Black box with  $n$  input lines and  $2^n$  output lines
- Only one output is a 1 for any given input

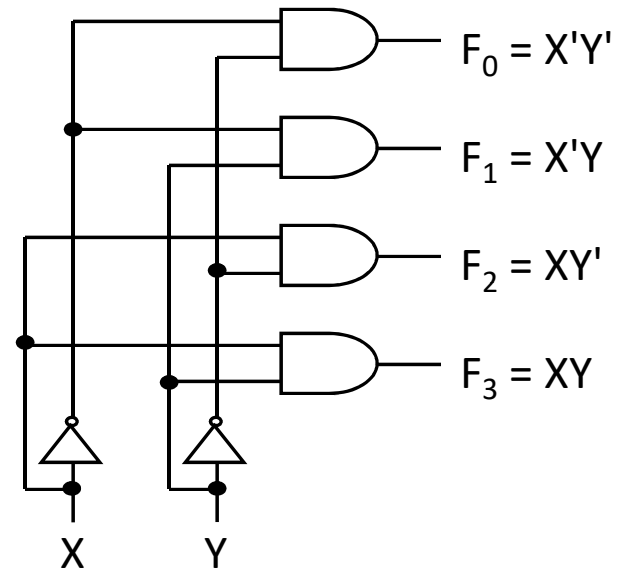
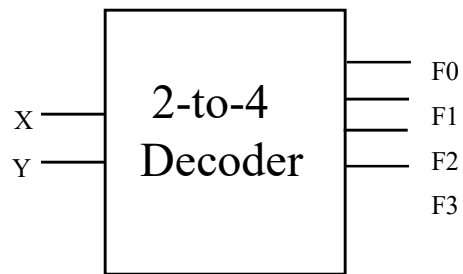


## 2-to-4 Binary Decoder

Truth Table:

X	Y	F <sub>0</sub>	F <sub>1</sub>	F <sub>2</sub>	F <sub>3</sub>
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

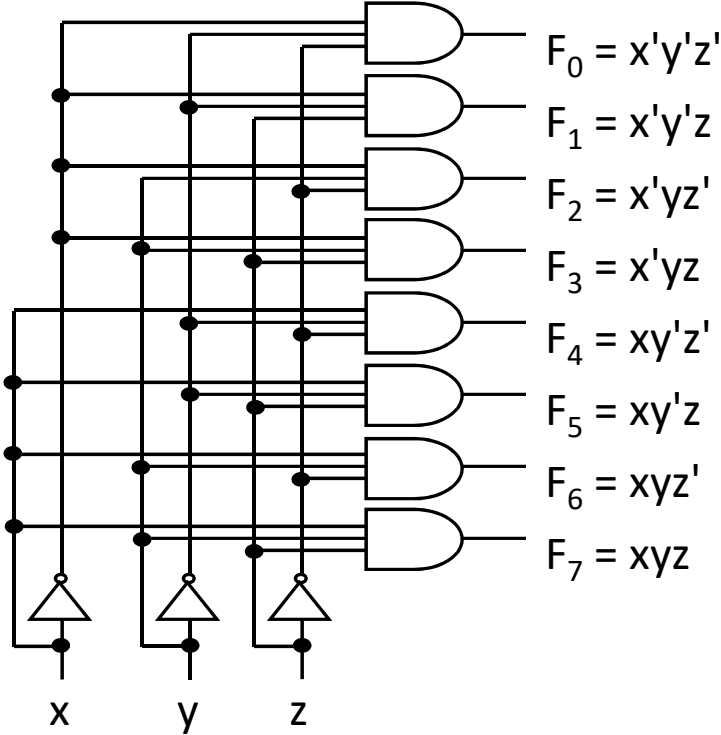
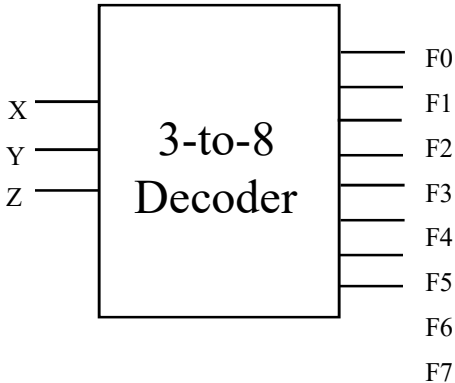
- From truth table, circuit for 2x4 decoder is:
- Note: Each output is a 2-variable minterm ( $X'Y'$ ,  $X'Y$ ,  $XY'$  or  $XY$ )



# 3-to-8 Binary Decoder

Truth Table:

x	y	z	F <sub>0</sub>	F <sub>1</sub>	F <sub>2</sub>	F <sub>3</sub>	F <sub>4</sub>	F <sub>5</sub>	F <sub>6</sub>	F <sub>7</sub>
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	1	0	0	0	0
1	0	0	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	1	0	0
1	1	0	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	1



## Implementing Functions Using Decoders

- Any  $n$ -variable logic function can be implemented using a single  $n$ -to- $2^n$  decoder to generate the minterms
  - OR gate forms the sum.
  - The output lines of the decoder corresponding to the minterms of the function are used as inputs to the or gate.
- Any combinational circuit with  $n$  inputs and  $m$  outputs can be implemented with an  $n$ -to- $2^n$  decoder with  $m$  OR gates.
- Suitable when a circuit has many outputs, and each output function is expressed with few minterms.

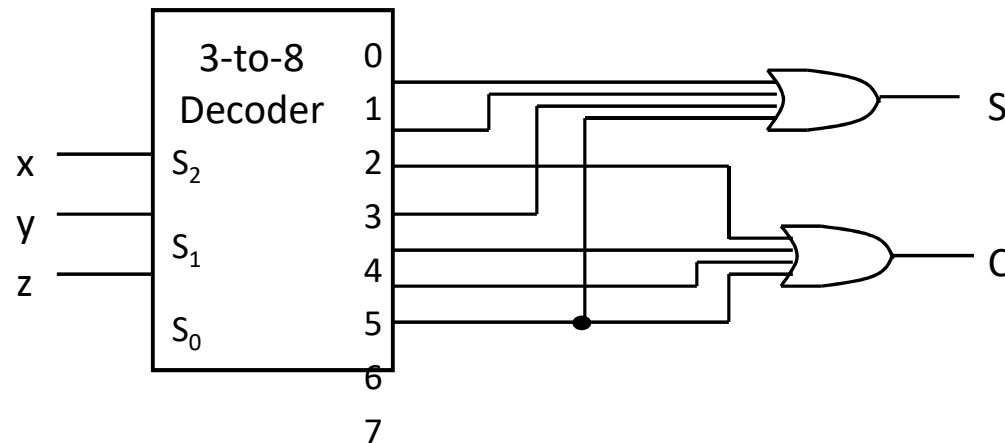
# Implementing Functions Using Decoders

- Example: Full adder

$$S(x, y, z) = S(1, 2, 4, 7)$$

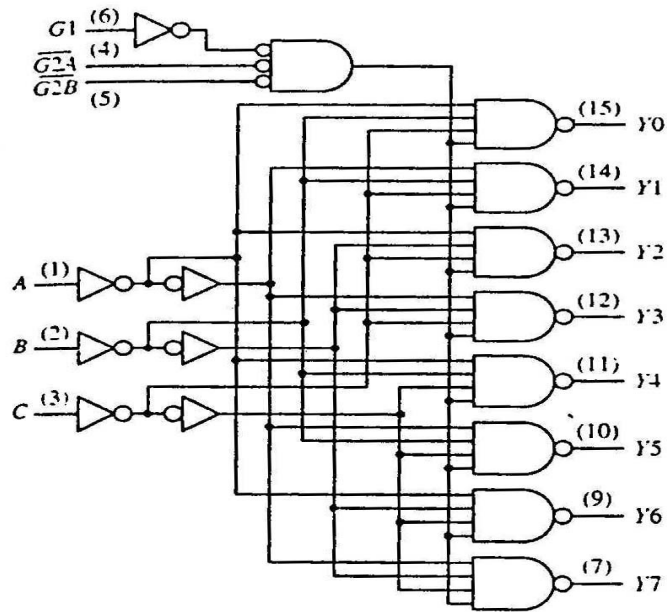
$$C(x, y, z) = S(3, 5, 6, 7)$$

x	y	z	C	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1



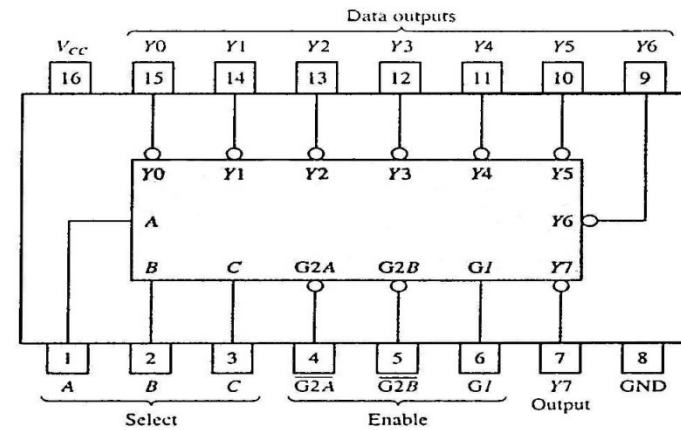
# Standard MSI Binary Decoders Example

## 74138 (3-to-8 decoder)



(a)

(a) Logic circuit.



(b)

(b) Package pin configuration.

Inputs					Outputs							
Enable		Select			Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
G1	$\overline{G2^*}$	C	B	A								
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L
x	H	x	x	x	H	H	H	H	H	H	H	H
L	x	x	x	x	H	H	H	H	H	H	H	H

$$\overline{G2^*} = \overline{G2A} + \overline{G2B}$$

(c)

(c) Function table.



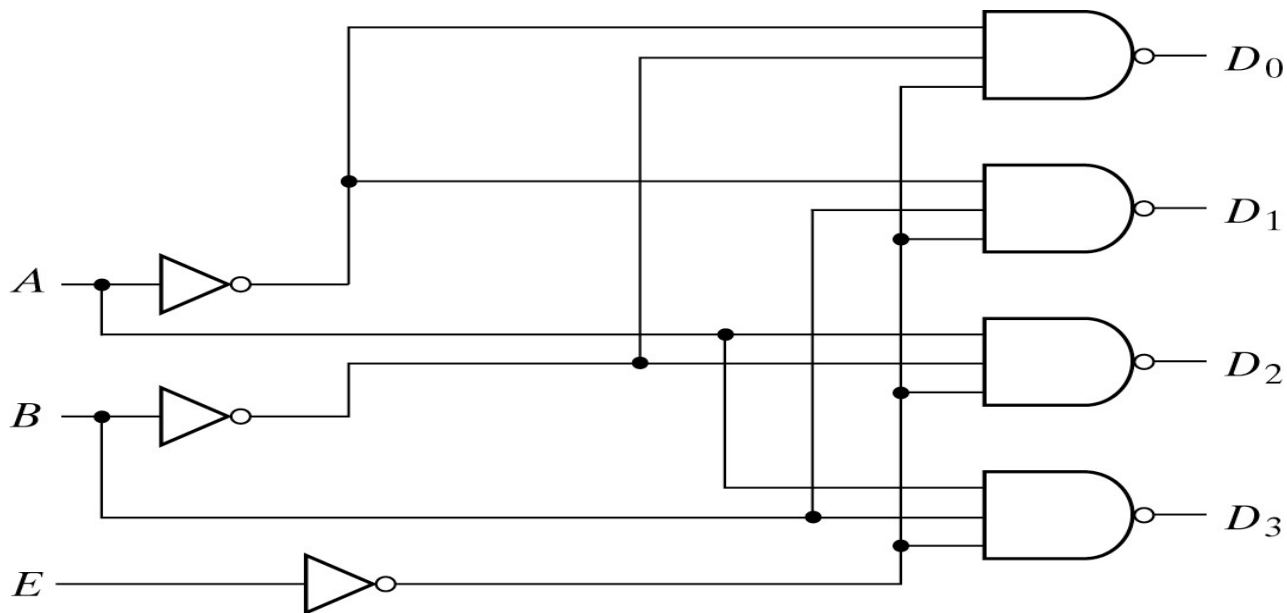
## Building a Binary Decoder with NAND Gates

- Start with a 2-bit decoder
  - Add an enable signal (E)

Note: use of NANDs

only one 0 active!

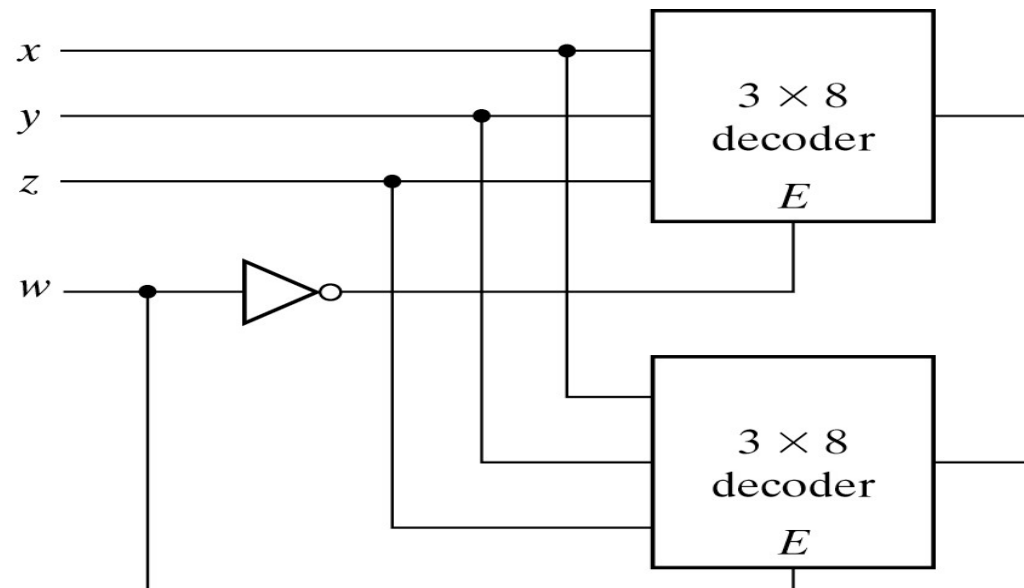
if E = 0



<i>E</i>	<i>A</i>	<i>B</i>
1	<i>X</i>	<i>X</i>
0	0	0
0	0	1
0	1	0
0	1	1

## Use two 3 to 8 decoders to make 4 to 16 decoder

- Enable can also be active high
- In this example, only one decoder can be active at a time.
- $x, y, z$  effectively select output line for  $w$



## Summary

- Decoder allows for generation of a single binary output from an input binary code
  - For an  $n$ -input binary decoder there are  $2^n$  outputs
- Decoders are widely used in storage devices (e.g. memories)
  - We will discuss these in a few weeks