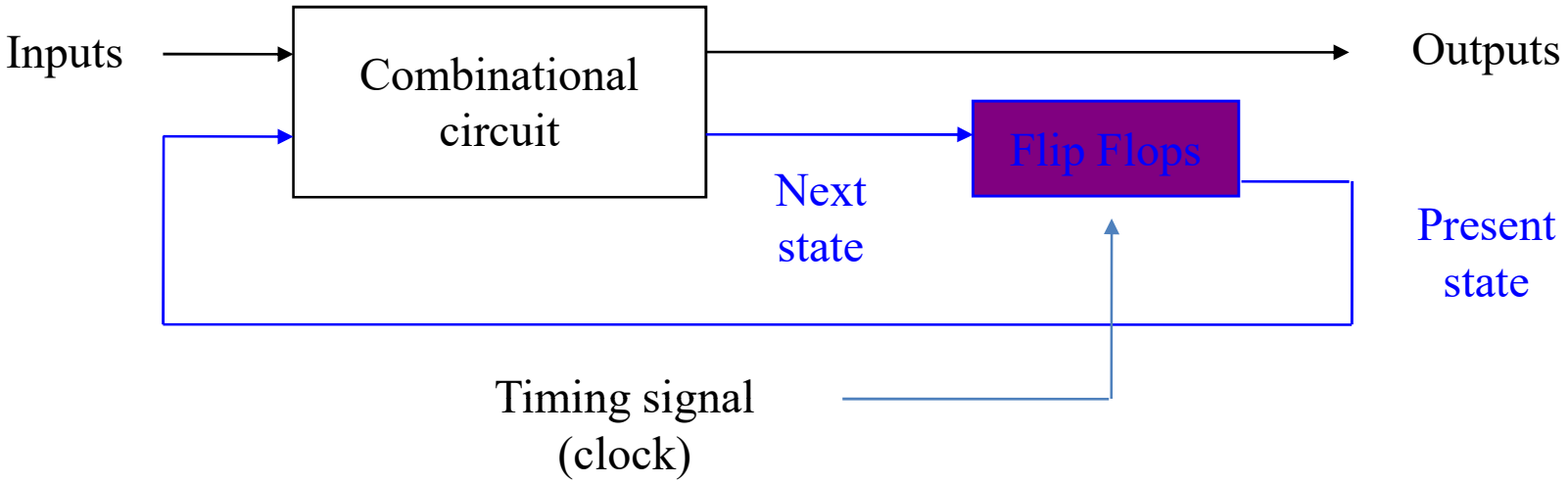
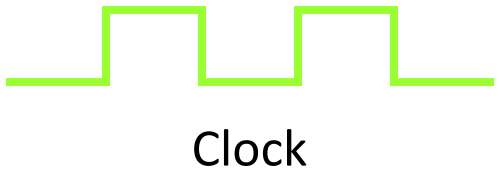
Sequential Circuit(D-Latch & D-Flip Flop)

Sequential Circuits



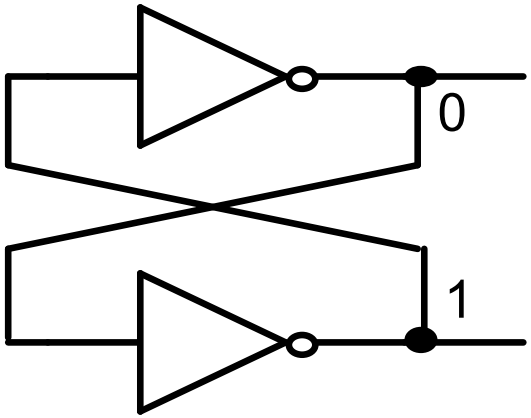
Clock
a periodic external event (input)



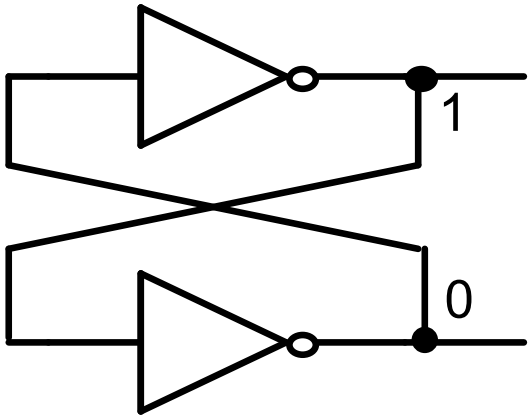
synchronizes when current state changes happen
keeps system well-behaved
makes it easier to design and build large systems

Cross-coupled Inverters

A stable value can be stored at inverter outputs



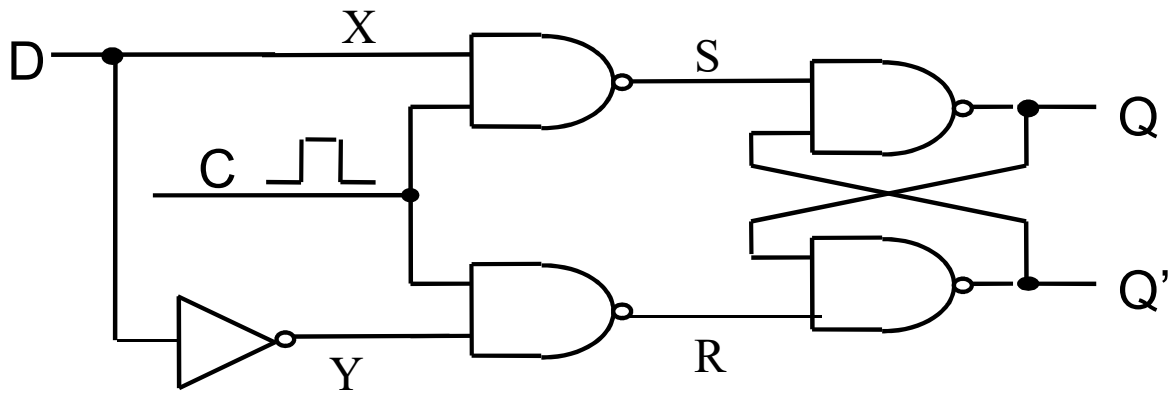
State 1



State 2

D Latch

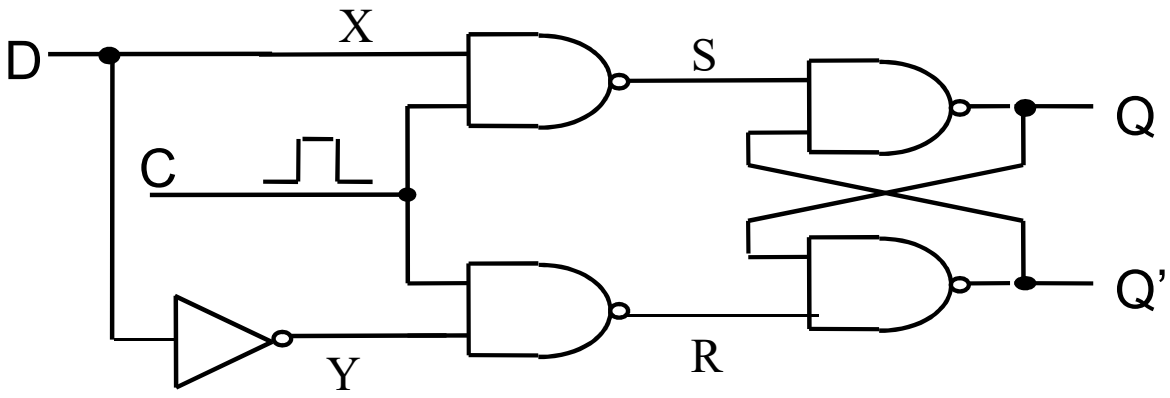
Q_o indicates the previous state (the previously stored value)



D	C	Q	Q'
0	1	0	1
1	1	1	0
X	0	Q_0	Q_0'

X	Y	C	Q	Q'	
0	0	1	Q_0	Q_0'	Store
0	1	1	0	1	Reset
1	0	1	1	0	Set
1	1	1	1	1	Disallowed
X	X	0	Q_0	Q_0'	Store

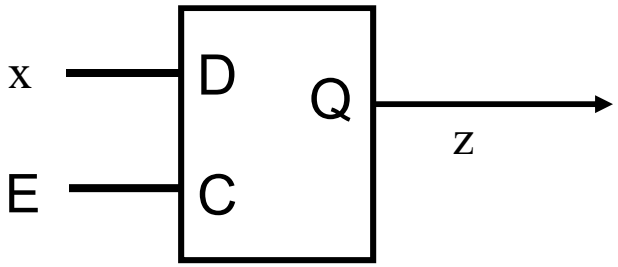
D Latch

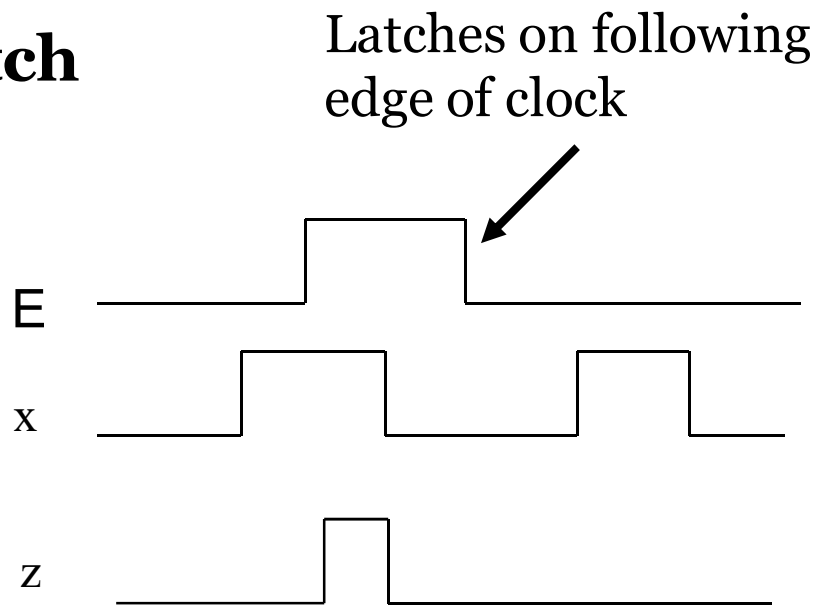


D	C	Q	Q'
0	1	0	1
1	1	1	0
X	0	Q_0	Q_0'

Input value D is passed to output Q when C is high
Input value D is ignored when C is low

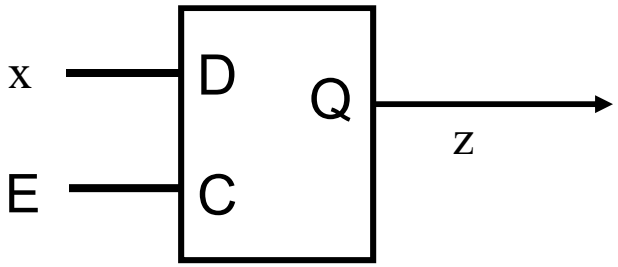
D Latch

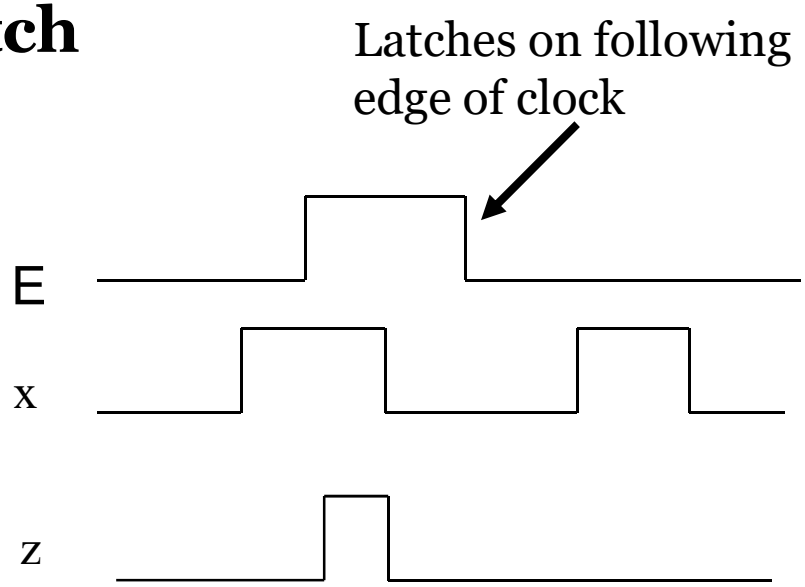




Z only changes when E is high
If E is high, Z will follow X

D Latch

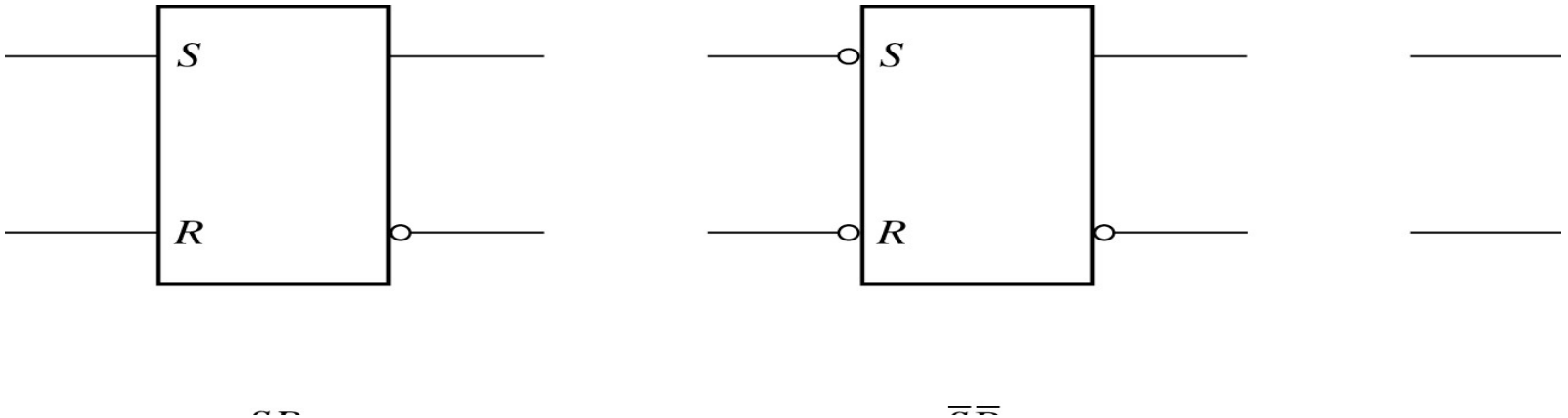




The D latch stores data indefinitely, regardless of input D values, if C = 0

Forms basic storage element in computers

Symbols for Latches



SR latch is based on NOR gates
S'R' latch based on NAND gates
D latch can be based on either.
D latch sometimes called transparent latch

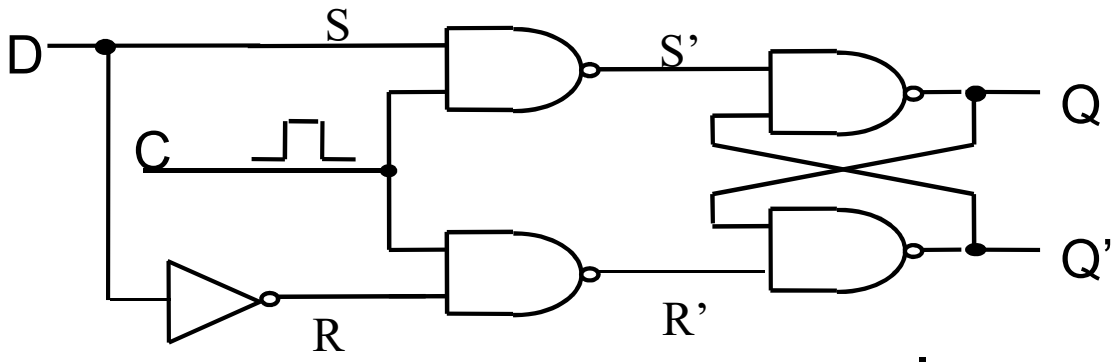
Summary

- With additional gates, an S-R latch can be converted to a D latch (D stands for data)
- D latch is simple to understand conceptually
  - When C = 1, data input D stored in latch and output as Q
  - When C = 0, data input D ignored and previous latch value output at Q

Overview

- Latches respond to trigger levels on control inputs
  - Example: If G = 1, input reflected at output
- Difficult to precisely time when to store data with latches
- Flip flips store data on a rising or falling trigger edge.
  - Example: control input transitions from 0 -> 1, data input appears at output
  - Data remains stable in the flip flop until until next rising edge.
- Different types of flip flops serve different functions
- Flip flops can be defined with characteristic functions.

D Latch



D	C	Q	Q'
0	1	0	1
1	1	1	0
X	0	Q_0	Q_0'

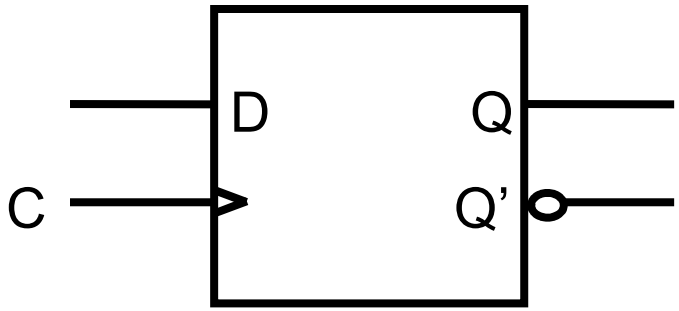
S	R	C	Q	Q'	
0	0	1	Q_0	Q_0'	Store
0	1	1	0	1	Reset
1	0	1	1	0	Set
1	1	1	1	1	Disallowed
X	X	0	Q_0	Q_0'	Store

When C is high, D passes from input to output (Q)

Clocking Event

What if the output only changed on a C transition?

Positive edge triggered



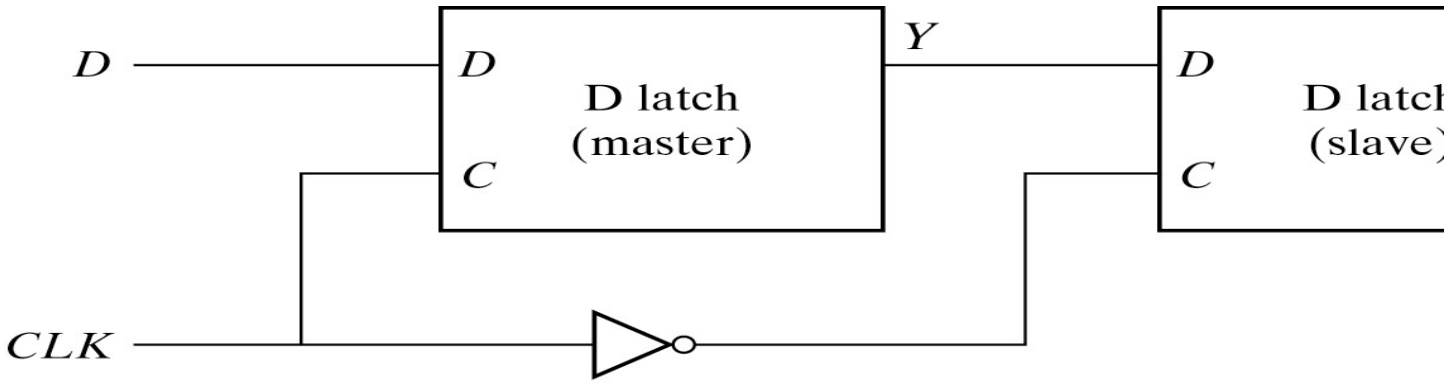
D	C	Q	Q'
0	↑	0	1
1	↑	1	0
X	0	Q_0	Q_0'

Hi-Lo edge

Lo-Hi edge

Master-Slave D Flip Flop

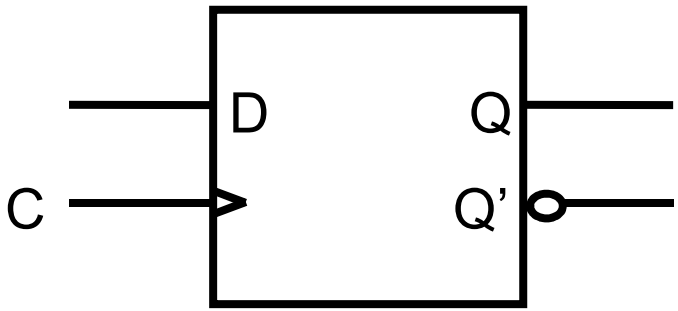
Consider two latches combined together
Only one *C* value active at a time
Output changes on falling edge of the clock



D Flip-Flop

Stores a value on the positive edge of *C*
Input changes at other times have no effect on output

Positive edge triggered

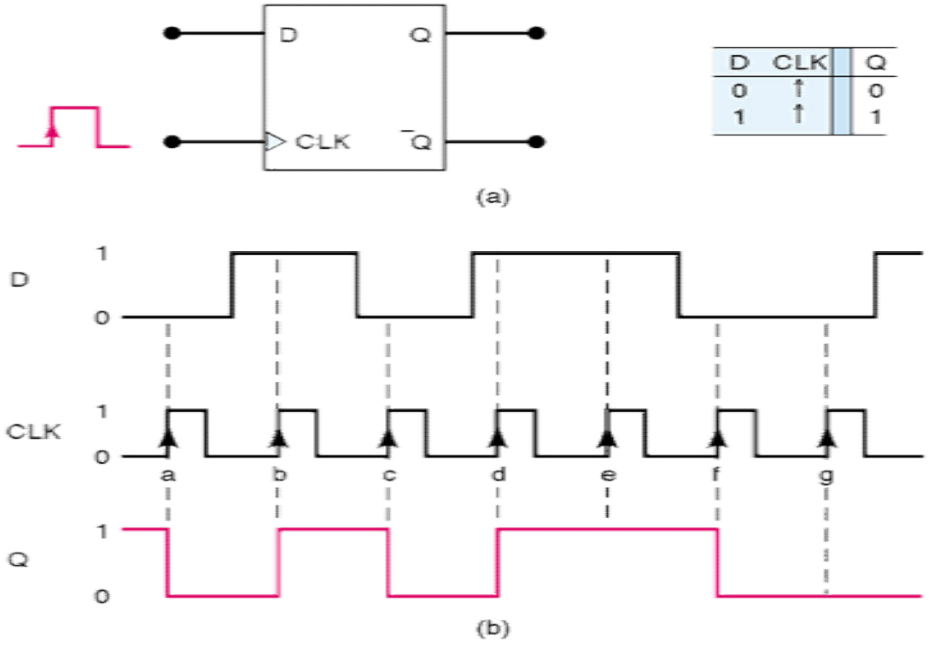


D	C	Q	Q'
0	↑	0	1
1	↑	1	0
X	0	Q_0	Q_0'

D gets latched to Q on the rising edge of the clock.

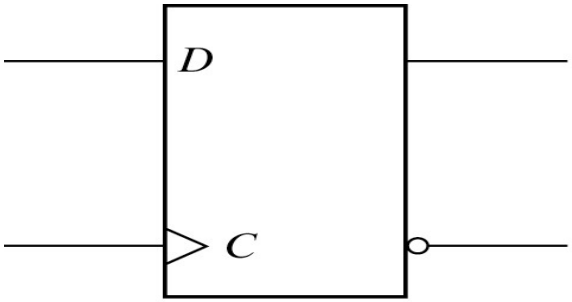
Clocked D Flip-Flop

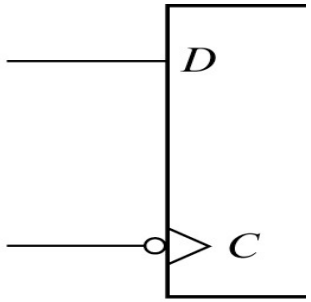
Stores a value on the positive edge of *C*
Input changes at other times have no effect on output



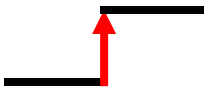
Positive and Negative Edge D Flip-Flop

D flops can be triggered on positive or negative edge
Bubble before *Clock (C)* input indicates negative edge trigger





(a) Positive edge (a) Negati



Lo-Hi edge

Hi-Lo edge

Summary

- Flip flops are powerful storage elements
  - They can be constructed from gates and latches!
- D flip flop is simplest and most widely used
- Asynchronous inputs allow for clearing and presetting the flip flop output
- Multiple flops allow for data storage
  - The basis of computer memory!
- Combine storage and logic to make a computation circuit

THANK YOU