

Sequential Circuit Excitation Table and Flip-Flop Conversion

Flip-Flop Excitation Tables

Present State	Next State	F.F. Input
$Q(t)$	$Q(t+1)$	D
0	0	0
0	1	1
1	0	0
1	1	1

Present State	Next State	F.F. Input
$Q(t)$	$Q(t+1)$	J K
0	0	0 x
0	1	1 x
1	0	x 1
1	1	x 0

0 0 (No change)

0 1 (Reset)

1 0 (Set)

1 1 (Toggle)

0 1 (Reset)

1 1 (Toggle)

0 0 (No change)

1 0 (Set)

Present State	Next State	F.F. Input
$Q(t)$	$Q(t+1)$	S R
0	0	0 x
0	1	1 0
1	0	0 1
1	1	x 0

$Q(t)$	$Q(t+1)$	T
0	0	0
0	1	1
1	0	1
1	1	0

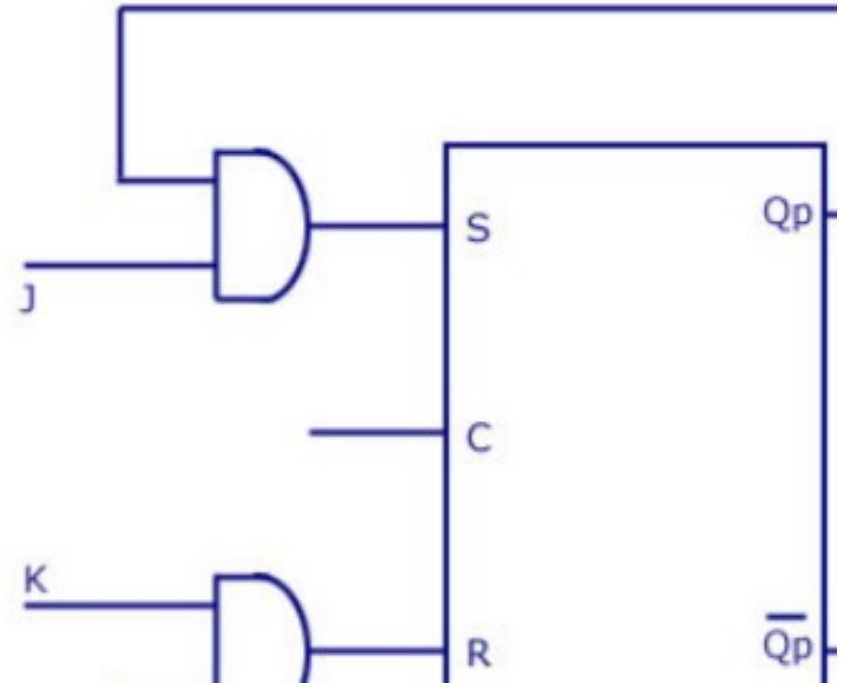


S-R Flip-Flop TO J-K Flip-Flop

Conversion Table

J-K Inputs		Outputs		S-R Inputs
J	K	Q _p	Q _{p+1}	S
0	0	0	0	0
0	0	1	1	X
0	1	0	0	0
0	1	1	0	0
1	0	0	1	1
1	1	0	1	1

Logic Diagram



		KQ _p		
	J	00	01	11
0		0 ⁰	X ¹	0 ³
1		1 ⁴	X ⁵	0 ⁷

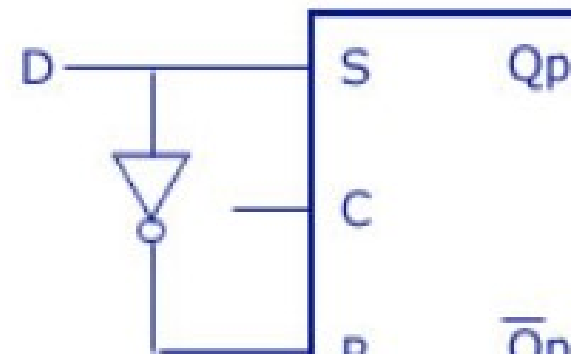
		KQ _p			
	J	00	01	11	10
0		X ⁰	0 ¹	1 ³	X ²
1		0 ⁴	0 ⁵	1 ⁷	0 ⁶

S-R Flip-Flop TO D Flip-Flop

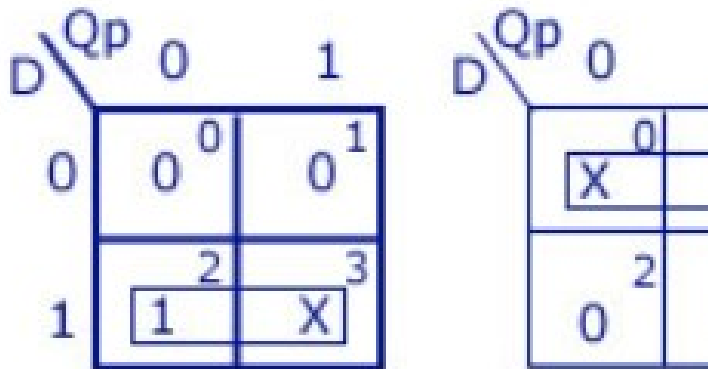
Conversion Table

D Input	Outputs		S-R Inj
	Q_p	Q_{p+1}	S
0	0	0	0
0	1	0	0
1	0	1	1

Logic Diagram



K-maps

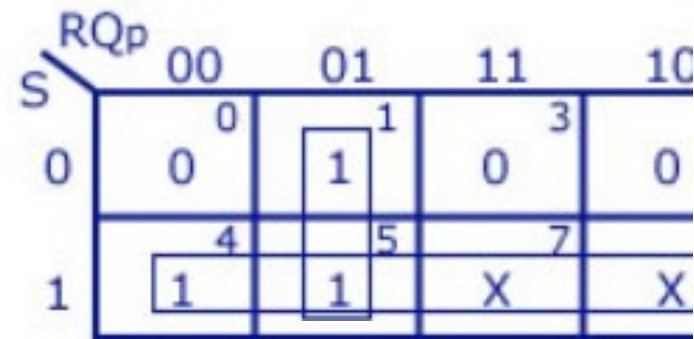


D Flip-Flop To S-R Flip Flop

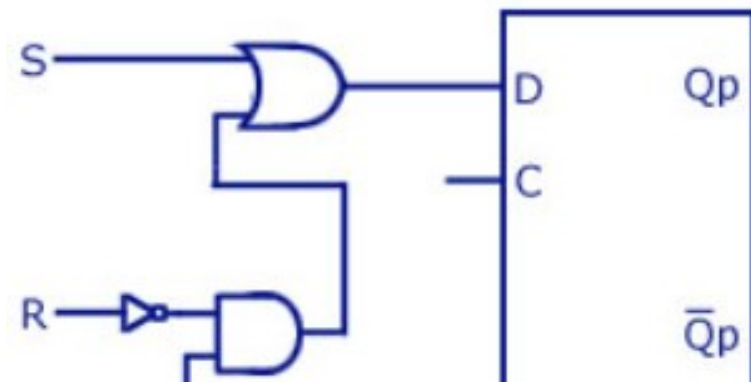
Conversion Table

S-R Inputs		Outputs		D Input
S	R	Q_p	Q_{p+1}	
0	0	0	0	0
0	0	1	1	1
0	1	0	0	0
0	1	1	0	0
1	0	0	1	1
1	0	1	1	1

K-map



Logic Diagram

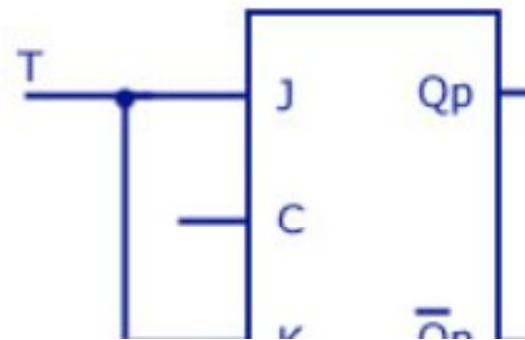


J-K Flip-Flop To T Flip-Flop

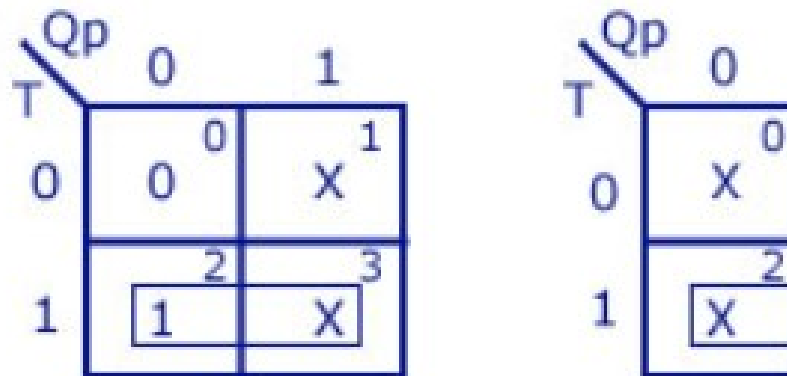
Conversion Table

T Input	Outputs		J-K Inp
	Q_p	Q_{p+1}	J
0	0	0	0
0	1	1	X
1	0	1	1

Logic Diagram



K-maps



D Flip-Flop To J-K Flip-Flop

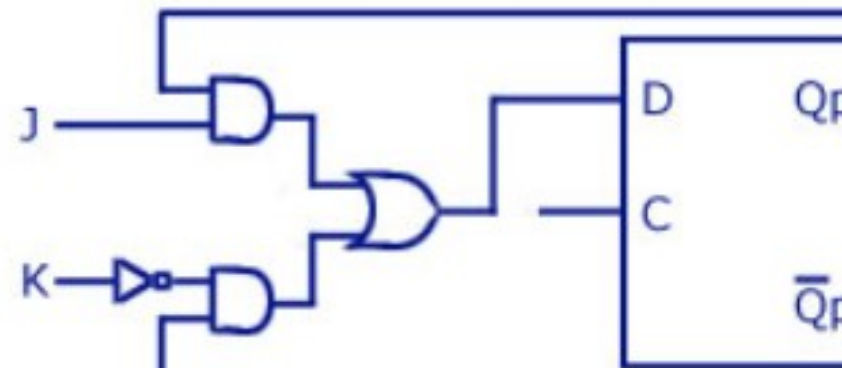
Conversion Table

J-K Input		Outputs		D Input
J	K	Q_p	Q_{p+1}	
0	0	0	0	0
0	0	1	1	1
0	1	0	0	0
0	1	1	0	0
1	0	0	1	0
1	0	1	1	1

K-map

J \ KQp	Qp			
	00	01	11	10
0	0	1	0	0
1	1	1	0	1

Logic Diagram

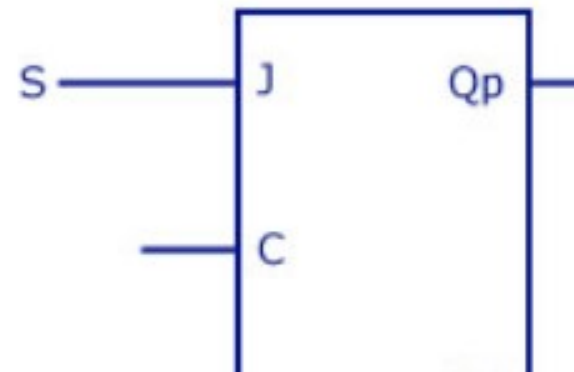


J-K Flip-Flop to S-R Flip-Flop

Conversion Table

S-R Inputs		Outputs		J-K Inputs	
S	R	Q _p	Q _{p+1}	J	K
0	0	0	0	0	0
0	0	1	1	X	X
0	1	0	0	0	1
0	1	1	0	X	1
1	0	0	1	1	0
1	0	1	1	X	X

Logic Diagram



		RQ _p		
		00	01	11
S	0	0 ⁰	X ¹	X ³
	1	1 ⁴	X ⁵	X ⁷

		RQ _p		
		00	01	11
S	0	X ⁰	0 ¹	1 ³
	1	X ⁴	0 ⁵	X ⁷