## Sequential Circuit (Asynchronous Counter Design)

## Asyn. Counters with MOD no. < $\mathbf{2}^{\text {n }}$

-States may be skipped resulting in a truncated sequence.
-Technique: force counter to recycle before going through all of the states in the binary sequence.
-Example: Given the following circuit, determine the counting sequence (and hence the modulus no.)

All J, K
inputs are
1 (HIGH).


## Cont...

-Example (cont'd):

All J, K inputs are 1 (HIGH).


MOD-6 counter produced by clearing (a MOD-8 binary counter) when count of six (110) occurs.

## Asyn. Counters with MOD no. < $\mathbf{2}^{\text {n }}$

Example (cont'd): Counting sequence of circuit (in CBA order).


## Asyn. Counters with MOD no. $<\mathbf{2}^{\text {n }}$

- Exercise: How to construct an asynchronous MOD-5 counter? MOD-7 counter? MOD-12 counter?
- Question: The following is a MOD-? counter?



## Asyn. Counters with MOD no. < $\mathbf{2}^{\mathbf{n}}$

- Decade counters (or BCD counters) are counters with 10 states (modulus-10) in their sequence. They are commonly used in daily life (e.g.: utility meters, odometers, etc.).
- Design an asynchronous decade counter.



## Asyn. Counters with MOD no. $<\mathbf{2}^{\text {n }}$

- Asynchronous decade/BCD counter (cont'd).



## Asynchronous Down Counters

- So far we are dealing with up counters. Down counters, on the other hand, count downward from a maximum value to zero, and repeat.
- Example: A 3-bit binary (MOD-2 ${ }^{3}$ ) down counter.



## Asynchronous Down Counters

- Example: A 3-bit binary (MOD-8) down counter.


| $Q_{2}$ | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- |

## Cascading Asynchronous Counters

- Larger asynchronous (ripple) counter can be constructed by cascading smaller ripple counters.
- Connect last-stage output of one counter to the clock input of next counter so as to achieve higher-modulus operation.
- Example: A modulus-32 ripple counter constructed from a modulus-4 counter and a modulus- 8 counter.



## Cascading Asynchronous Counters

- Example: A 6-bit binary counter (counts from o to 63) constructed from two 3-bit counters.


| $A_{5}$ | $A_{4}$ | $A_{3}$ | $A_{2}$ | $A_{1}$ | $A_{0}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 0 | $\vdots$ | $\vdots$ | $\vdots$ |
| 0 | 0 | 0 | 1 | 1 | 1 |
| 0 | 0 | 1 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 | 1 |
| $:$ | $:$ | $:$ | $:$ | $:$ | $:$ |

## Cascading Asynchronous Counters

- If counter is a not a binary counter, requires additional output.
- Example: A modulus-100 counter using two decade counters.

$T C=1$ when counter recycles to 0000

