Sequential Circuit (Register \& Counter)

## Parallel In/Serial Out Shift Registers

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Logic symbol

## Parallel In/Parallel Out Shift Registers

- Simultaneous input and output of all data bits.



## Bidirectional Shift Registers

- Data can be shifted either left or right, using a control line $R I G H T / \overline{L E F T}$ (or simply RIGHT) to indicate the direction.



## Bidirectional Shift Registers

- 4-bit bidirectional shift register with parallel load.



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- 4-bit bidirectional shift register with parallel load.

| Mode Control |  |  |
| :---: | :---: | :---: |
| $s_{1}$ | $s_{0}$ | Register Operation |
| 0 | 0 | No change |
| 0 | 1 | Shift right |
| 1 | 0 | Shift left |
| 1 | 1 | Parallel load |

## An Application - Serial Addition

- Most operations in digital computers are done in parallel. Serial operations are slower but require less equipment.
- A serial adder is shown below. $A \leftarrow A+B$.



## An Application - Serial Addition

- $A=0100 ; B=0111 . A+B=1011$ is stored in $A$ after 4 clock pulses.

| Initial: | $\begin{aligned} & A: 010 \underline{0} \\ & B: 0111 \end{aligned}$ | $Q: \underline{0}$ |
| :---: | :---: | :---: |
| Step 1: $0+1+0$ | A: $101 \underline{0}$ | $Q: 0$ |
| Step 2 $\begin{aligned} & S=1, c=0 \\ & 0+1+0 \\ & s=1, c=0 \end{aligned}$ | $\begin{aligned} & B: \times 011 \\ & A: 1101 \\ & B \cdot x \times 01 \end{aligned}$ | $Q: \underline{0}$ |
| Step 3: $1+1+0$ $S=0, C=1$ | $\begin{aligned} & A: 011 \underline{0} \\ & B: x x \times 0 \end{aligned}$ | $Q: \underline{1}$ |
| $\begin{aligned} \text { Step 4: } & 0+0+1 \\ & S=1, C=0 \end{aligned}$ | $\begin{aligned} & A: 1011 \\ & B: x x x x \end{aligned}$ | $Q: \underline{0}$ |

## Shift Register Counters

- Shift register counter: a shift register with the serial output connected back to the serial input.
- They are classified as counters because they give a specified sequence of states.
- Two common types: the Johnson counter and the Ring counter.


## Ring Counters

- One flip-flop (stage) for each state in the sequence.
- The output of the last stage is connected to the D input of the first stage.
- An $n$-bit ring counter cycles through $n$ states.
- No decoding gates are required, as there is an output that corresponds to every state the counter is in.


## Ring Counters

- Example: A 6-bit (MOD-6) ring counter.


| Clock | $Q_{0}$ | $Q_{1}$ | $Q_{2}$ | $Q_{3}$ | $Q_{4}$ | $Q_{5}$ |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: |
| $\longrightarrow 0$ | 1 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 | 0 | 0 | 0 |
| 2 | 0 | 0 | 1 | 0 | 0 | 0 |
| 3 | 0 | 0 | 0 | 1 | 0 | 0 |
| 4 | 0 | 0 | 0 | 0 | 1 | 0 |
| 5 | 0 | 0 | 0 | 0 | 0 | 1 |



## Johnson Counters

- The complement of the output of the last stage is connected back to the D input of the first stage.
- Also called the twisted-ring counter.
- Require fewer flip-flops than ring counters but more flipflops than binary counters.
- An $n$-bit Johnson counter cycles through $2 n$ states.
- Require more decoding circuitry than ring counter but less than binary counters.


## Cont...

- Example: A 4-bit (MOD-8) Johnson counter.


| C Io c k | $Q_{0}$ | $Q_{1}$ | $Q_{2}$ | $Q_{3}$ |
| :--- | :---: | :---: | :---: | :---: |
| $\longrightarrow 0$ | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 |
| 2 | 1 | 1 | 0 | 0 |
| 3 | 1 | 1 | 1 | 0 |
| 4 | 1 | 1 | 1 | 1 |
| 5 | 0 | 1 | 1 | 1 |
| 6 | 0 | 0 | 1 | 1 |
| 7 | 0 | 0 | 0 | 1 |



## Cont...

- Decoding logic for a 4-bit Johnson counter.

| Clock | $A$ | $B$ | $C$ | $D$ | Decoding |
| :--- | :---: | :---: | :---: | :---: | :---: |
| $\longrightarrow 0$ | 0 | 0 | 0 | 0 | $A^{\prime} \cdot D^{\prime}$ |
| 1 | 1 | 0 | 0 | 0 | $A . B^{\prime}$ |
| 2 | 1 | 1 | 0 | 0 | $B . C^{\prime}$ |
| 3 | 1 | 1 | 1 | 0 | $C . D^{\prime}$ |
| 4 | 1 | 1 | 1 | 1 | $A . D^{\prime}$ |
| 5 | 0 | 1 | 1 | 1 | $A^{\prime} . B$ |
| 6 | 0 | 0 | 1 | 1 | $B^{\prime} . C$ |
| 7 | 0 | 0 | 0 | 1 | $C^{\prime} . D$ |



## THANK YOU

