

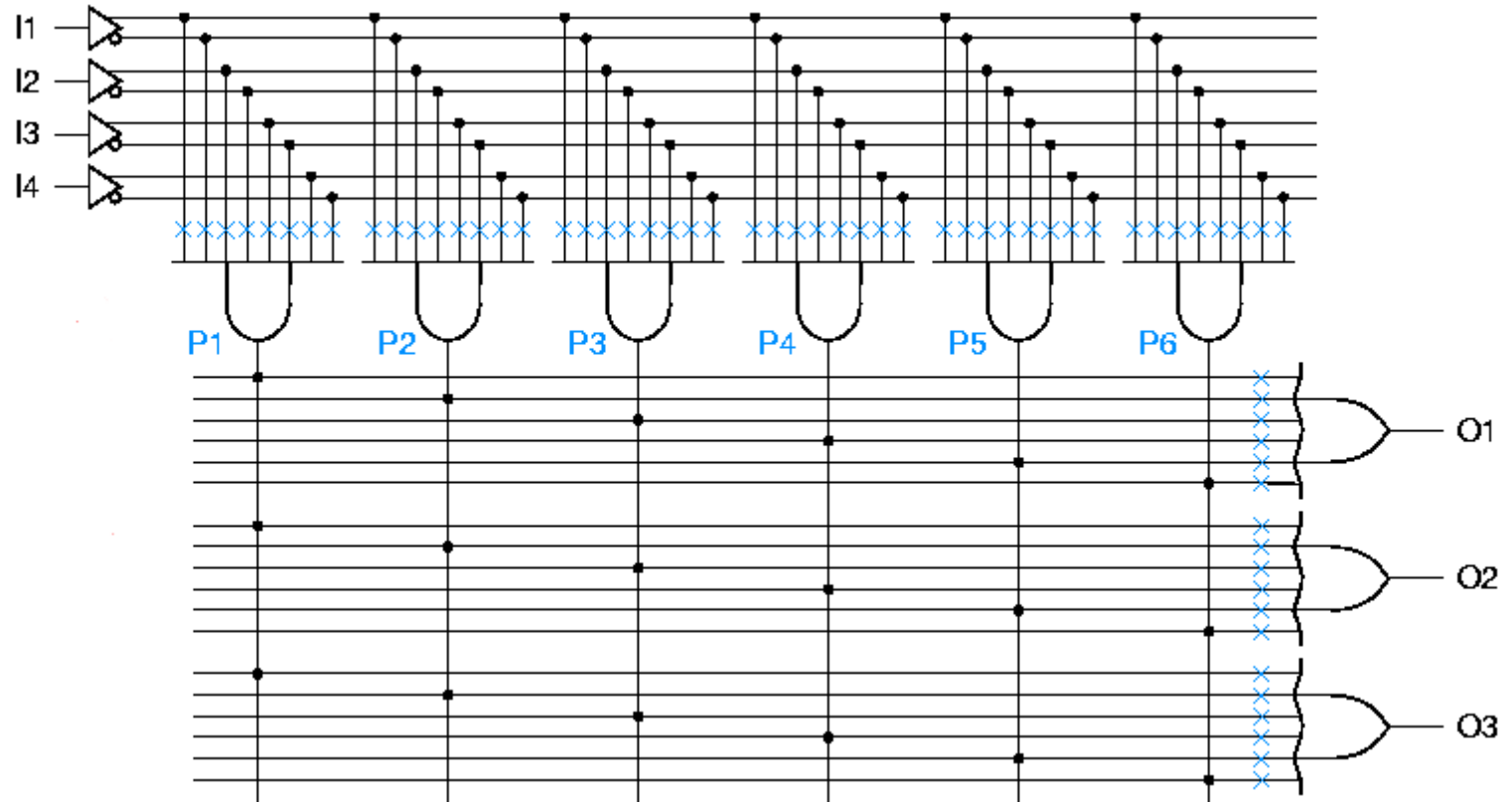
PLD

- The first PLDs were Programmable Logic Arrays (PLAs).
- A PLA is a combinational, 2-level AND-OR device that can be programmed to realise any sum-of-products logic expression.
- A PLA is limited by:
 - the number of inputs (n)
 - the number of outputs (m)
 - the number of product terms (p)
- We refer to an “ $n \times m$ PLA with p product terms”. Usually, $p \ll 2^n$.
- An $n \times m$ PLA with p product terms contains p $2n$ -input AND gates and m p -input OR gates.

PLD

- Each input is connected to a buffer that produces a true and a complemented version of the signal.

A 4x3 PLA with
6 product
terms.



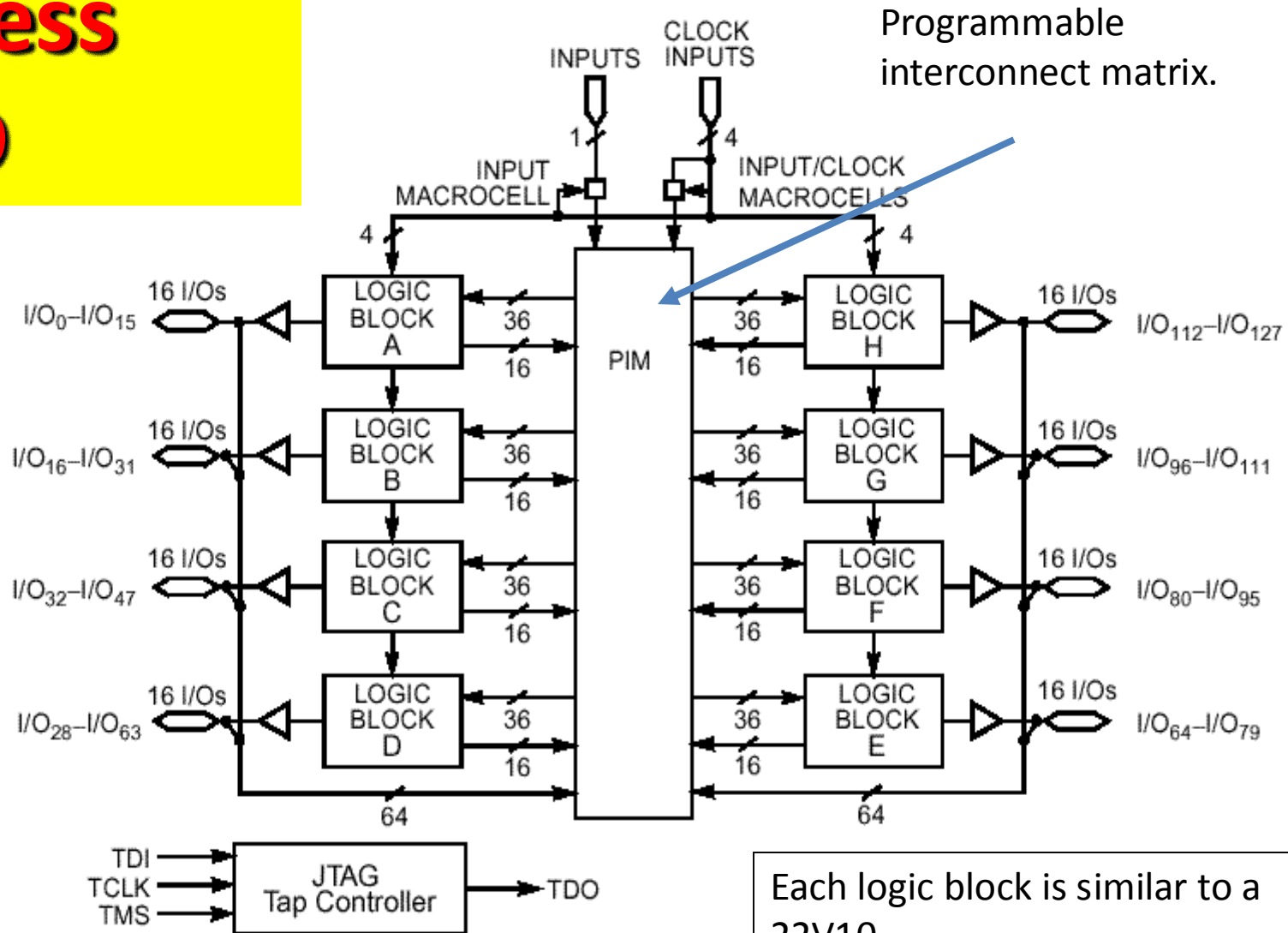
- Potential connections are indicated by Xs.
- The device is programmed by establishing the needed connections.
- The connections are made by fuses.

CPLD

Complex PLDs

- What is the next step in the evolution of programmable logic?
 - **More gates!**
- How do we get more gates?
-
- We could put several PALs on one chip and put an interconnection matrix between them!!
 - This is called a ***Complex PLD (CPLD)***.

Cypress CPLD



Logic block diagram

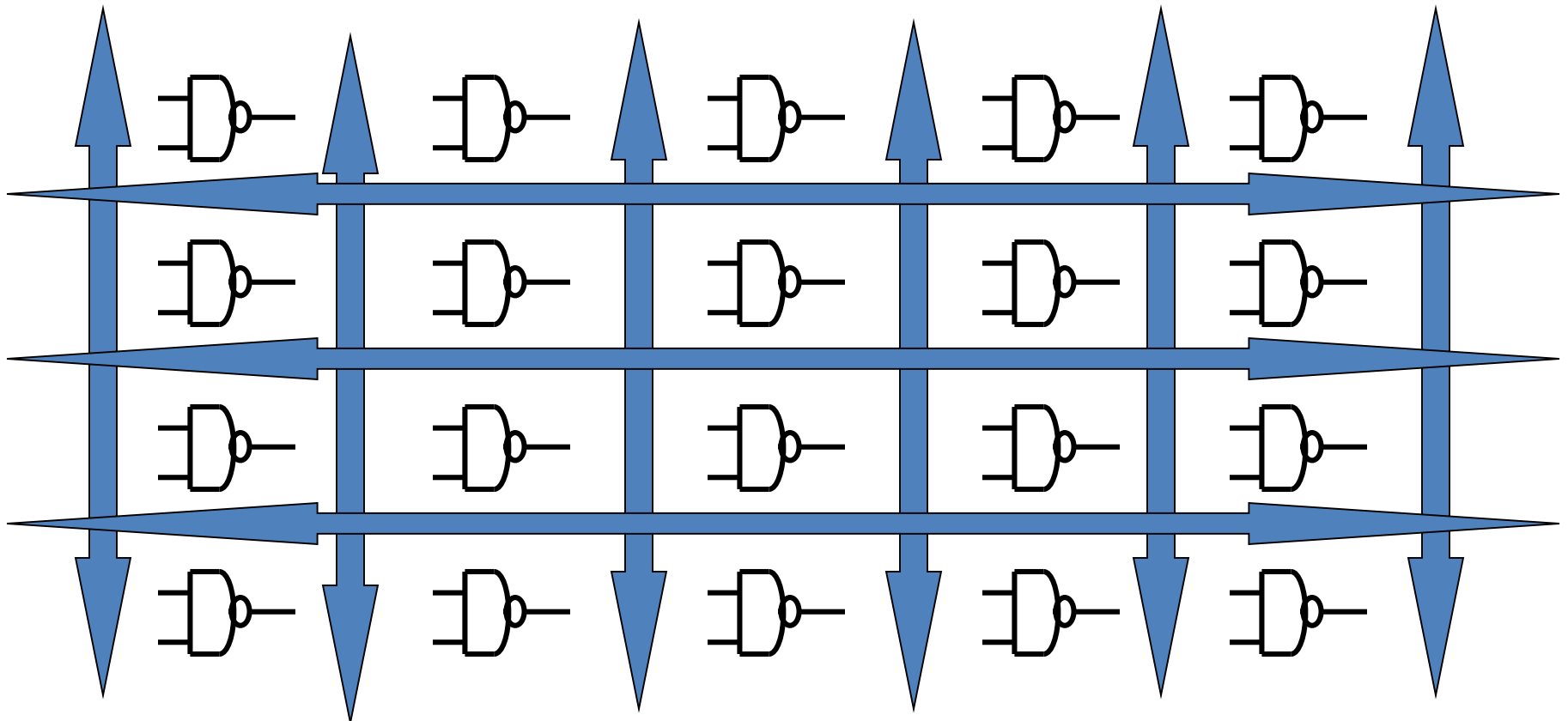
Figure 1. Ultra37128 Block Diagram

Cypress CPLDs

- Ultra37000 Family
 - 32 to 512 Macrocells
 - Fast (T_{pd} 5 to 10ns depending on number of macrocells)
 - Very good routing resources for a CPLD

Other approaches and Issues

- Another approach to building a “better” PLD is
 - place a lot of primitive gates on a die,
 - and then **place programmable interconnect** between them:



FPGA

What is an FPGA?

- Field Programmable Gate Array
- Fully programmable alternative to a customized chip
- Used to implement functions in hardware
- Also called a Reconfigurable Processing Unit (RPU)

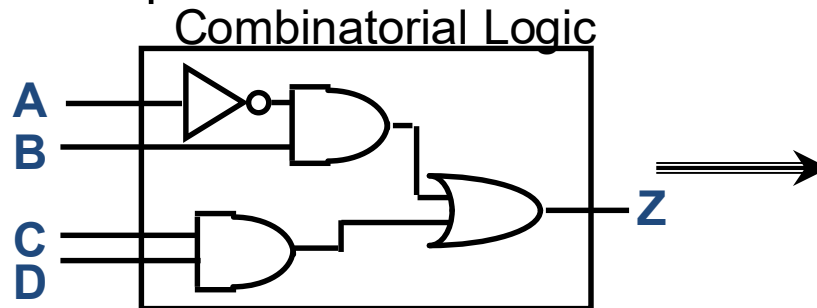
Reasons to use an FPGA

- Hardwired logic is very fast
- Can interface to outside world
 - Custom hardware/peripherals
 - “Glue logic” to custom co/processors
- Can perform **bit-level** and **systolic** operations not suited for traditional CPU/MPU

Look Up Tables

- Combinatorial Logic is stored in 16x1 SRAM Look Up Tables (LUTs) in a CLB

- Example:

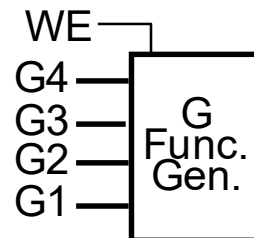


Look Up Table
4-bit address

A	B	C	D	Z
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

$$2^{(2^4)} = 64K !$$

- Capacity is limited by number of inputs, not complexity
- Choose to use each function generator as 4 input logic (LUT) or as high speed sync.dual port RAM



Field Programmable Gate Arrays

The FPGA approach to arrange primitive logic elements (logic cells) arrange in **rows/columns** with programmable routing between them.

What constitutes a primitive logic element?

Lots of different choices can be made! Primitive element must be classified as a “complete logic family”.

- A primitive gate like a **NAND gate**
- A **2/1 mux** (this happens to be a complete logic family)
- A **Lookup table** (i.e, 16x1 lookup table can implement any 4 input logic function).

Often combine one of the above with a DFF to form the primitive logic element.

Issues in FPGA Technologies

- Complexity of Logic Element
 - How many **inputs/outputs** for the logic element?
 - Does the basic logic element contain a **FF**? What **type**?
- Interconnect
 - How **fast** is it? Does it offer 'high speed' paths that cross the chip? How many of these?
 - Can I have on-chip **tri-state** busses?
 - **How routable** is the design? If 95% of the logic elements are used, can I route the design?
 - More routing means more **routability**, but less room for logic elements

Issues in FPGA Technologies (cont)

- **Macro elements**
 - Are there SRAM blocks? Is the SRAM dual ported?
 - Is there fast adder support (i.e. fast carry chains?)
 - Is there fast logic support (i.e. cascade chains)
 - What other types of macro blocks are available (fast decoders? register files?)
- **Clock support**
 - How many global clocks can I have?
 - Are there any on-chip Phase Logic Loops (PLLs) or Delay Locked Loops (DLLs) for clock synchronization, clock multiplication?

Issues in FPGA Technologies (cont)

- What type of **IO support** do I have?
 - TTL, CMOS are a given
 - Support for mixed 5V, 3.3v IOs?
 - 3.3 v internal, but 5V tolerant inputs?
 - Support for **new low voltage signaling standards**?
 - GTL+, GTL (Gunning Transceiver Logic) - used on Pentium II
 - HSTL - High Speed Transceiver Logic
 - SSTL - Stub Series-Terminate Logic
 - USB - IO used for Universal Serial Bus (differential signaling)
 - AGP - IO used for Advanced Graphics Port
 - Maximum number of IO? Package types?
 - Ball Grid Array (BGA) for high density IO

Altera FPGA Family

- **Altera Flex10K/10KE**
 - LEs (Logic elements) have 4-input LUTS (look-up tables) +1 FF
 - Fast Carry Chain between LE's, Cascade chain for logic operations
 - Large blocks of SRAM available as well
- **Altera Max7000/Max7000A**
 - EEPROM based, very fast (Tpd = 7.5 ns)
 - Basically a PLD architecture with programmable interconnect.
 - Max 7000A family is 3.3 v

Altera Flex 10K FPGA Family

Table 1. FLEX 10K Device Features

Feature	EPF10K10 EPF10K10A	EPF10K20	EPF10K30 EPF10K30A	EPF10K40	EPF10K50 EPF10K50V
Typical gates (logic and RAM), <i>Note (1)</i>	10,000	20,000	30,000	40,000	50,000
Usable gates	7,000 to 31,000	15,000 to 63,000	22,000 to 69,000	29,000 to 93,000	36,000 to 116,000
Logic elements (LEs)	576	1,152	1,728	2,304	2,880
Logic array blocks (LABs)	72	144	216	288	360
Embedded array blocks (EABs)	3	6	6	8	10
Total RAM bits	6,144	12,288	12,288	16,384	20,480
Maximum user I/O pins	134	189	246	189	310

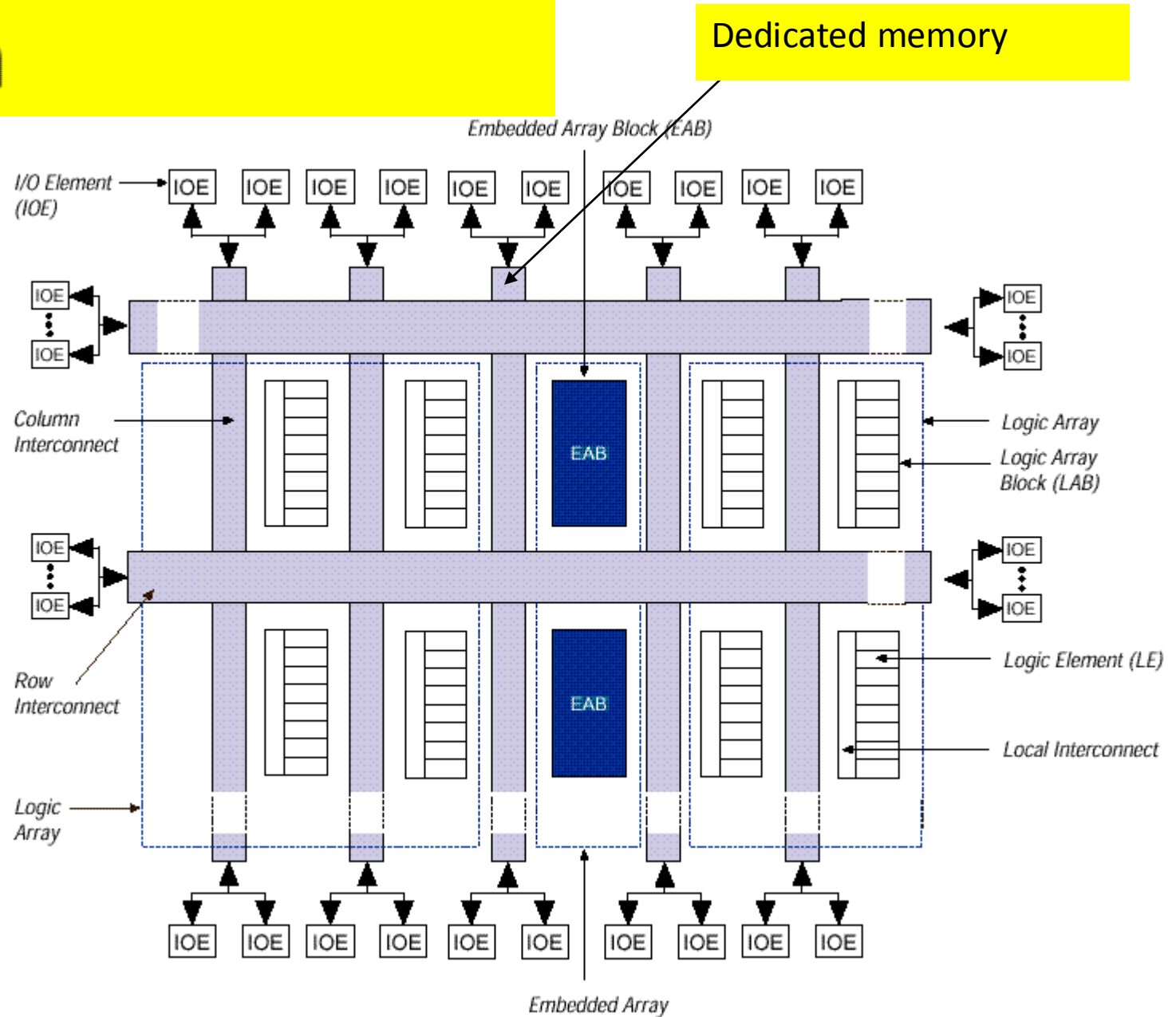
Altera Flex 10K FPGA Family (cont)

Feature	EPF10K70	EPF10K100 EPF10K100A	EPF10K130V	EPF10K250A
Typical gates (logic and RAM), <i>Note (1)</i>	70,000	100,000	130,000	250,000
Usable gates	46,000 to 118,000	62,000 to 158,000	82,000 to 211,000	149,000 to 310,000
LEs	3,744	4,992	6,656	12,160
LABs	468	624	832	1,520
EABs	9	12	16	20
Total RAM bits	18,432	24,576	32,768	40,960
Maximum user I/O pins	358	406	470	470

Note to tables:

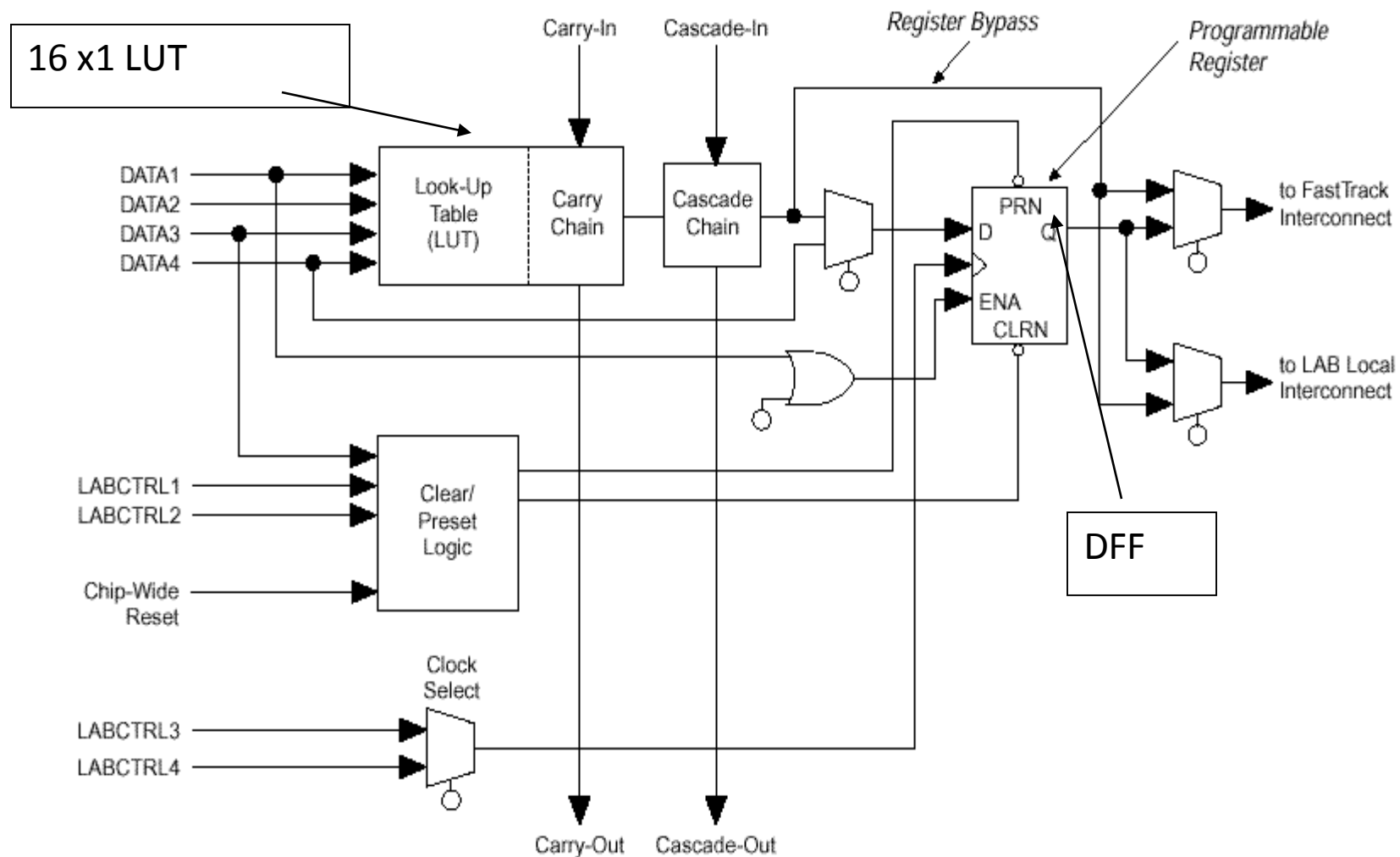
(1) For designs that require JTAG boundary-scan testing, the built-in JTAG circuitry contributes up to 31,250 additional

FLEX 10K Device Block Diagram



FLEX 10K Logic Element

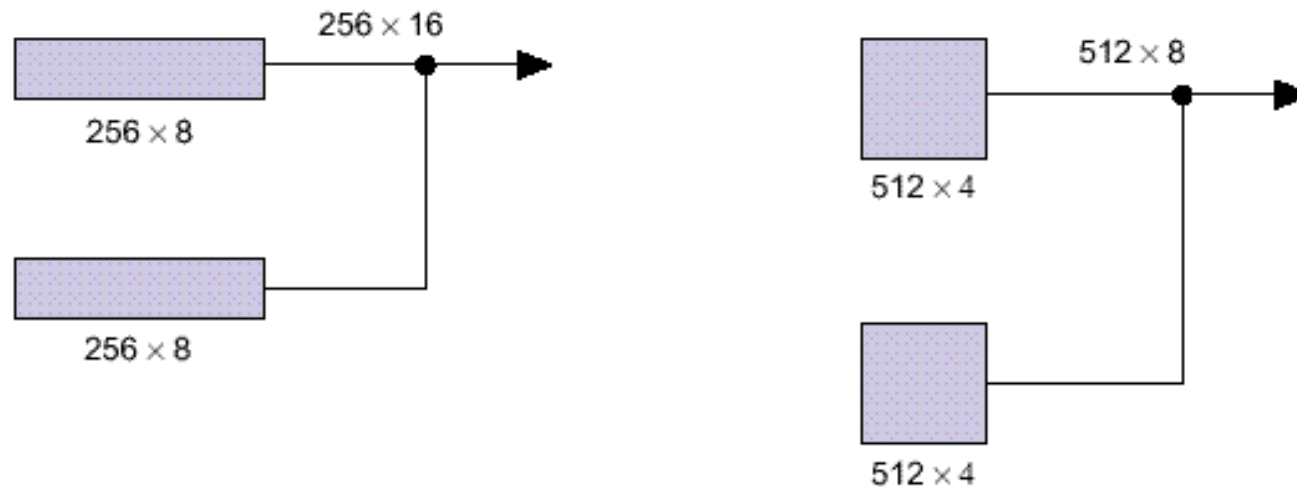
Figure 6. FLEX 10K Logic Element



Emedded Array Block

- Memory block, Can be configured:
 - 256×8 , 512×4 , 1024×2 , 2048×1

Figure 3. Examples of Combining EABs



Actel FPGA Family

- MXDS Family
 - **Fine grain** Logic Elements that contain Mux logic + DFF
 - Embedded **Dual Port SRAM**
 - **One Time Programmable** (OTP) - means that no configuration loading on powerup, no external serial ROM
 - **AntiFuse** technology for programming (AntiFuse means that you program the fuse to make the connection).
 - **Fast** (Tpd = 7.5 ns)
 - **Low density** compared to Altera, Xilinx - maximum number of gates is 36,000