

The slide features a central image of a Xilinx FPGA chip. Surrounding the chip are several circular icons representing different applications: a server rack, a car, a mobile phone, a handheld device, a keyboard, and a printer. The background is a light blue grid with the words 'High Performance', 'CoolClock', 'Low Power', and 'PowerCache' written in a stylized, glowing font. The title 'FPGA Design Flow' is centered in a bold, dark blue font.

FPGA Design Flow

FPGA Design process (1)

Design and implement a simple unit permitting to speed up encryption with RC5-similar cipher with fixed key set on 8031 microcontroller. Unlike in the experiment 5, this time your unit has to be able to perform an encryption algorithm by itself, executing 32 rounds.....



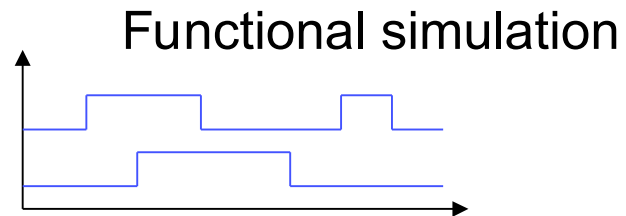
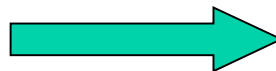
Specification / Pseudocode

On-paper hardware design
(Block diagram & ASM chart)

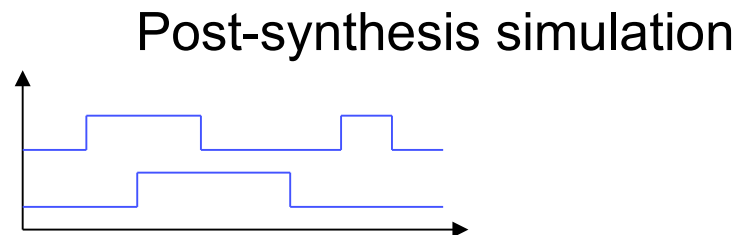
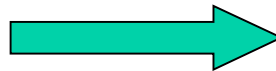
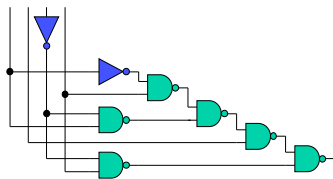


VHDL description (Your Source Files)

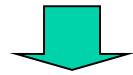
```
Library IEEE;  
use ieee.std_logic_1164.all;  
use ieee.std_logic_unsigned.all;  
  
entity RCS_core is  
  port(  
    clock, reset, encr_decr: in std_logic;  
    data_input: in std_logic_vector(31 downto 0);  
    data_output: out std_logic_vector(31 downto 0);  
    out_full: in std_logic;  
    key_input: in std_logic_vector(31 downto 0);  
    key_read: out std_logic;  
  );  
end AES_core;
```



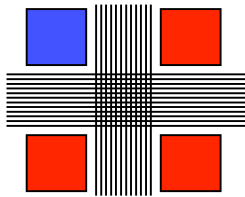
Synthesis



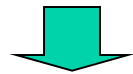
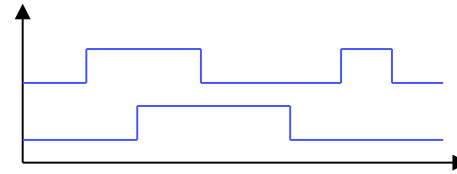
FPGA Design process (2)



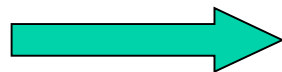
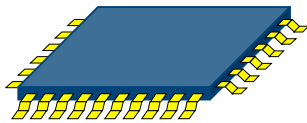
Implementation



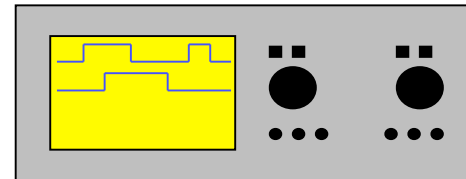
Timing simulation



Configuration



On chip testing



Tools used in FPGA Design Flow

