



# Session 1.1

## INTRODUCTION TO VLSI DESIGN

# OVERVIEW OF DIGITAL DESIGN USING VERILOG

- Evolution of Computer-Aided Digital Design
- Emergence of HDLs
- Typical Design Flow
- Design Methodologies
- Importance of HDLs
- Popularity of Verilog HDL

# EVOLUTION OF COMPUTER-AIDED DIGITAL DESIGN

- SSI: Small scale integration
  - A few gates on a chip
- MSI: Medium scale integration
  - Hundreds of gates on a chip
- LSI: Large scale integration
  - Thousands of gates on a chip
  - CAD: Computer-Aided Design
  - Logic and circuit simulators
  - Prototyping on bread board
  - Layout by hand (on paper or a computer terminal)

# EVOLUTION OF COMPUTER-AIDED DIGITAL DESIGN (CONT'D)

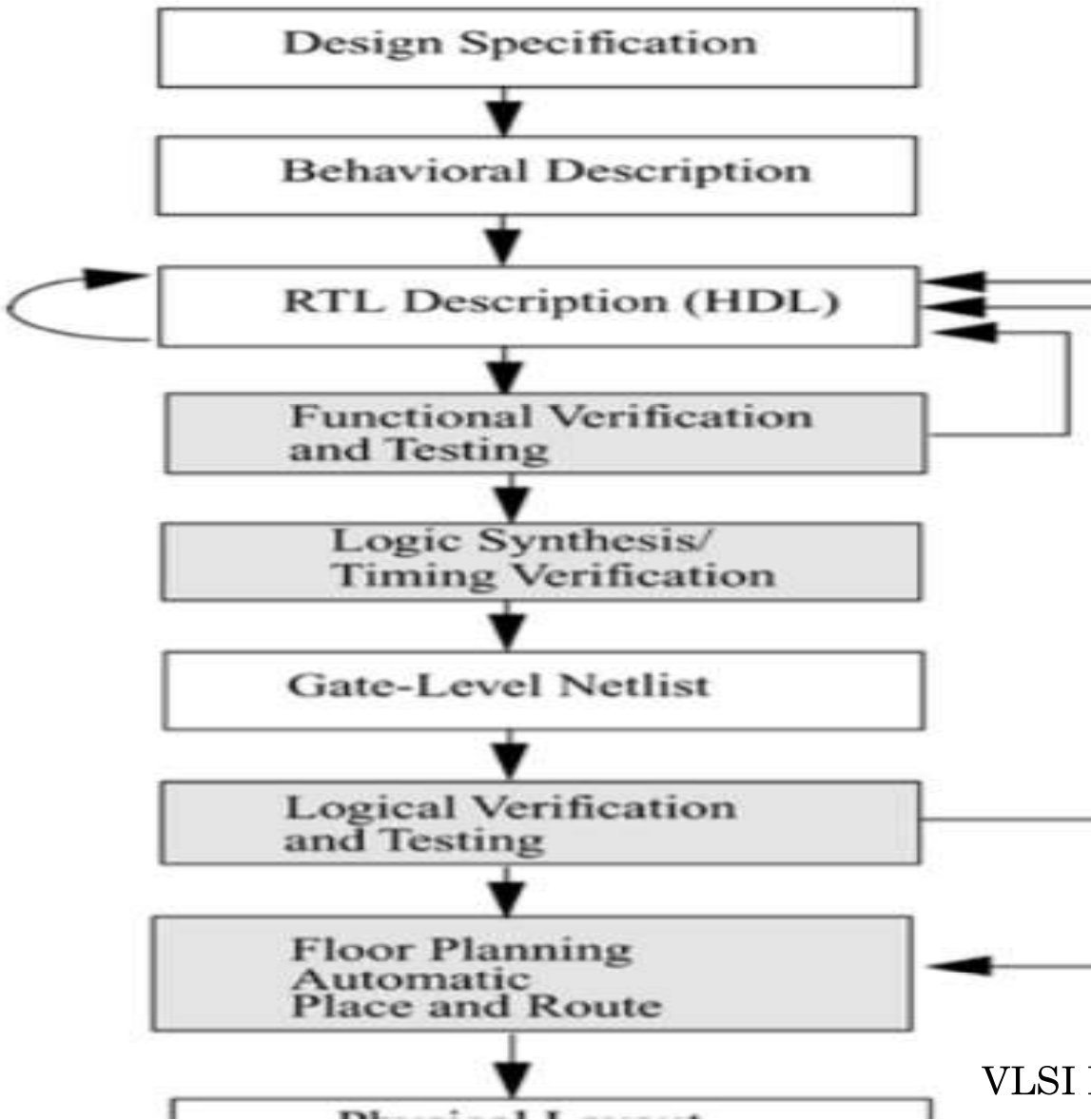
- VLSI: Very Large Scale Integration
  - Hundred thousands of gates
  - Not feasible anymore:
    - Bread boarding
    - Manual layout design
  - Simulator programs
  - Automatic place-and-route
  - Bottom-Up design
    - Design small building blocks
    - Combine them to develop bigger ones
  - More and more emphasis on logic simulation

## EMERGENCE OF HDLS

- The need to a standardized language for hardware description
  - Verilog<sup>®</sup> and VHDL
- Simulators emerged
  - Usage: functional verification
  - Path to implementation: manual translation into gates
- Logic synthesis technology
  - Late 1980s
  - Dramatic change in digital design
    - Design at Register-Transfer Level (RTL) using an HDL

## VLSI IC DESIGN FLOW

1. Design specification
2. Behavioral description
3. RTL description
4. Functional verification and testing
5. Logic synthesis
6. Gate-level netlist
7. Logical verification and testing
8. Floor planning, automatic place & route
9. Physical layout
10. Layout verification
11. Implementation



VLSI IC Design Flow

