

VLSI IC DESIGN FLOW

✓ *Design specification*

- In any design, specifications are written first.
- Specifications describe abstractly the functionality, interface, and overall architecture of the digital circuit to be designed.
- At this point, the architects do not need to think about how they will implement this circuit.

✓ *Behavioral description*

- A behavioral description is then created to analyze the design in terms of functionality, performance, compliance to standards, and other high-level issues.
- Behavioral descriptions are often written with HDL

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✓ *RTL description*

- The behavioral description is manually converted to an RTL description in an HDL.
- The designer has to describe the data flow that will implement the desired digital circuit.
- From this point onward, the design process is done with the assistance of EDA tools

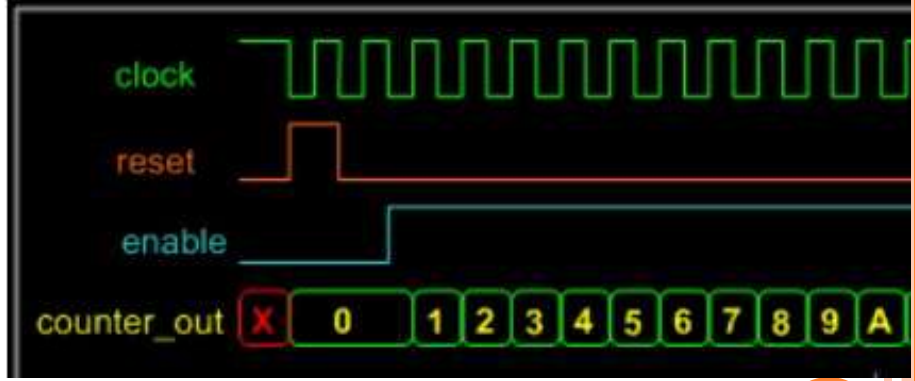
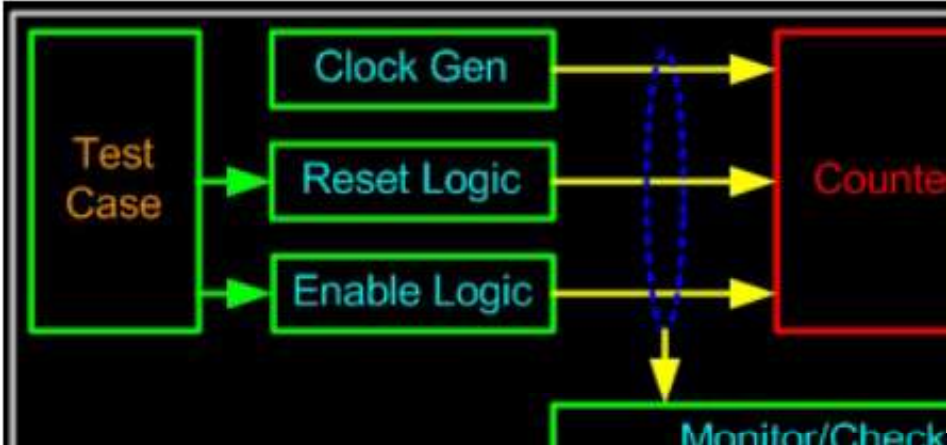
✓ *Functional verification and testing*

- Simulation is the process of verifying the functional characteristics of models at any level of abstraction.
- We use simulators to simulate the Hardware models.
- To test if the RTL code meets the functional requirements of the specification, we must see if all the RTL blocks are functionally correct.
- To achieve this we need to write a testbench

- RTL Description

```
1 module addbit (  
2 a      , // first input  
3 b      , // Second input  
4 ci     , // Carry input  
5 sum    , // sum output  
6 co     // carry output  
7 );  
8 //Input declaration  
9 input a;  
10 input b;  
11 input ci;  
12 //Output declaration  
13 output sum;  
14 output co;  
15 //Port Data types  
16 wire a;  
17 wire b;  
18 wire ci;  
19 wire sum;  
20 wire co;
```

- Functional Verification and Testing



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✓ *Logic Synthesis and Gate level Netlist*

- The Logic synthesis tools convert the RTL description to a gate-level netlist.
- A gate-level netlist is a description of the circuit in terms of gates and connections between them.
- Logic synthesis tools ensure that the gate-level netlist meets timing, area, and power specifications.

✓ *Logical verification and testing*

- After the synthesis there are a couple of things that are normally done before passing the netlist to backend (Place and Route)
 - ❖ **Formal Verification** : Check if the RTL to gate mapping is correct.
 - ❖ **Scan insertion** : Insert the scan chain in the case of ASIC.

SYNTHESIS FLOW

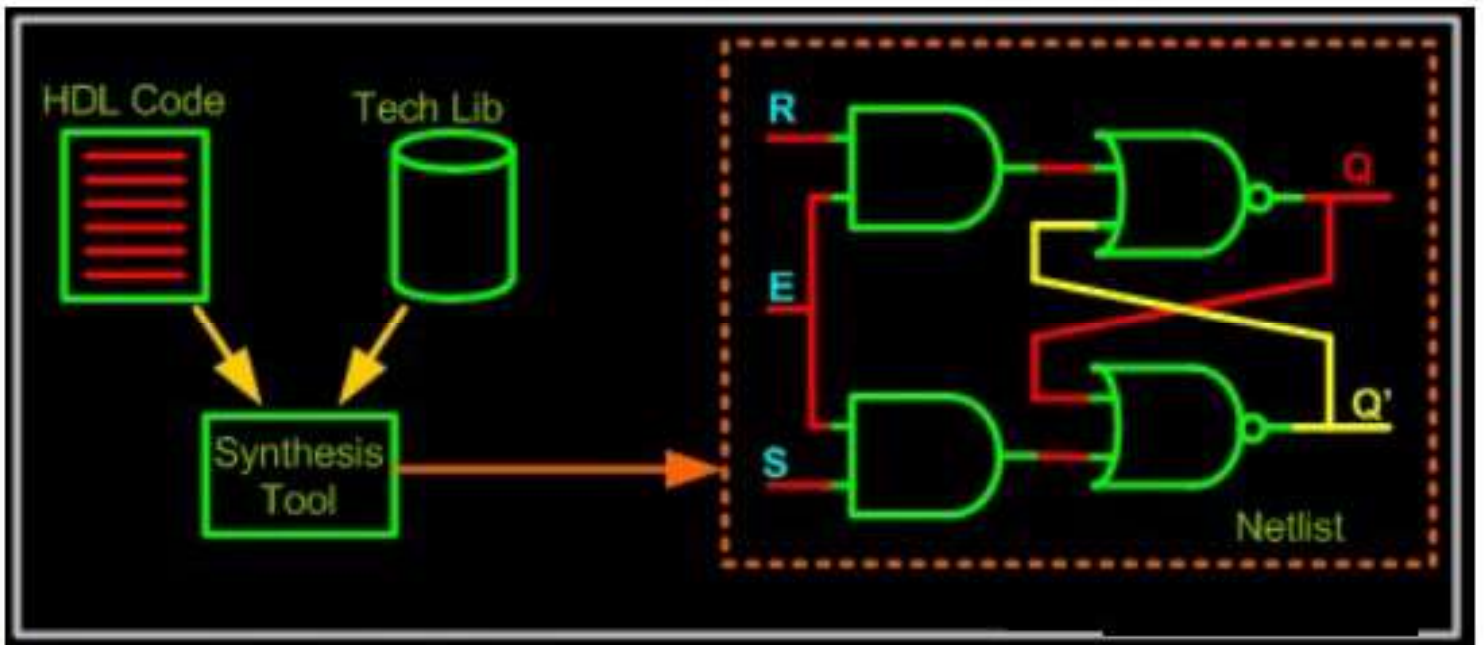


Figure : Synthesis Flow



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✓ ***Floor planning, automatic place & route***

- The gatelevel netlist from the synthesis tool is taken and imported into place and route tool in Verilog netlist format.
- All the gates and flip-flops are placed; clock tree synthesis and reset is routed.
- After this each block is routed.
- The P&R tool output is a GDS file, used by foundry for fabricating the ASIC

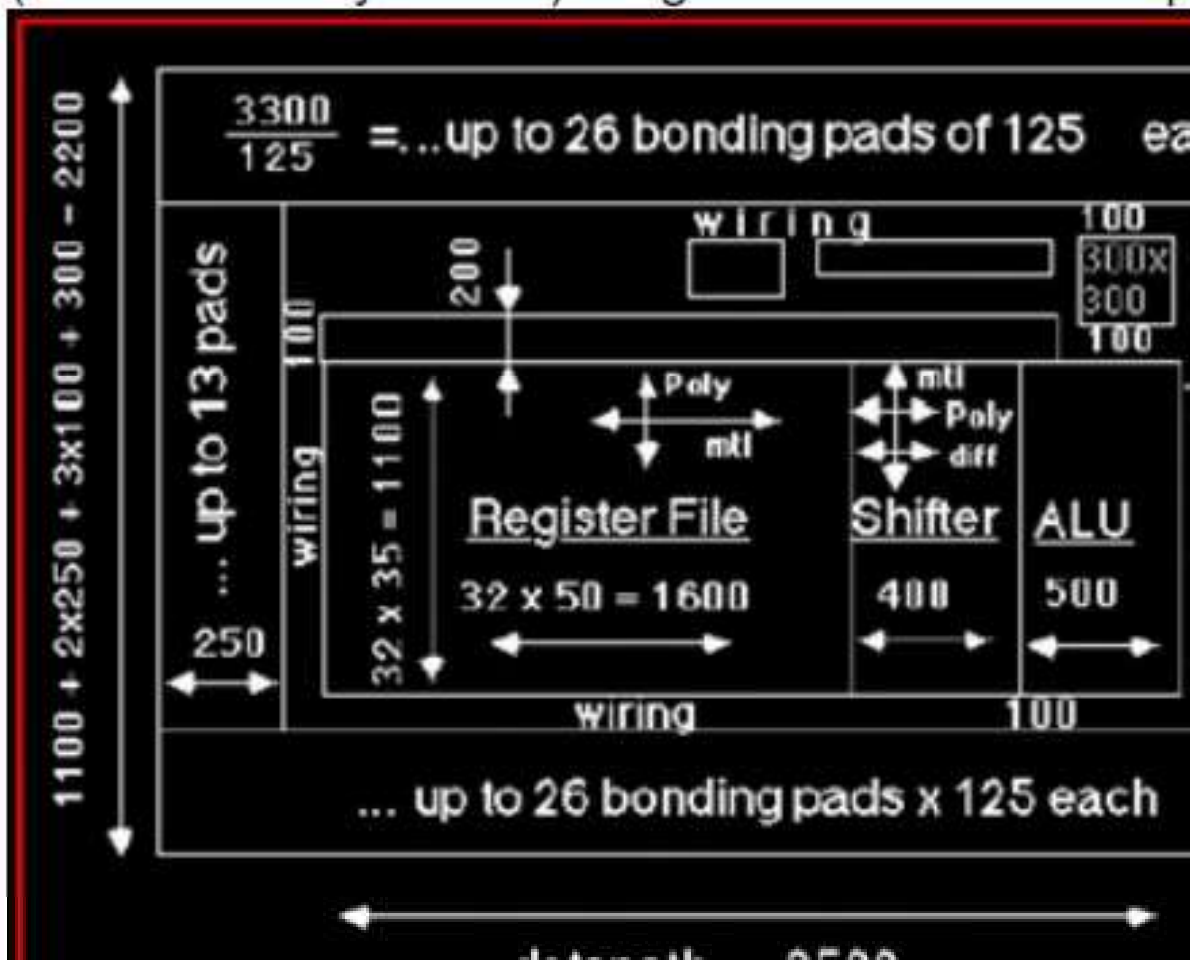
✓ ***Physical layout***

- The gate-level netlist is input to an Automatic Place and Route tool, which creates a layout.

✓ ***Layout verification and implementation***

- ✓ The layout is verified and then fabricated on a chip

PLACEMENT



FINAL LAYOUT

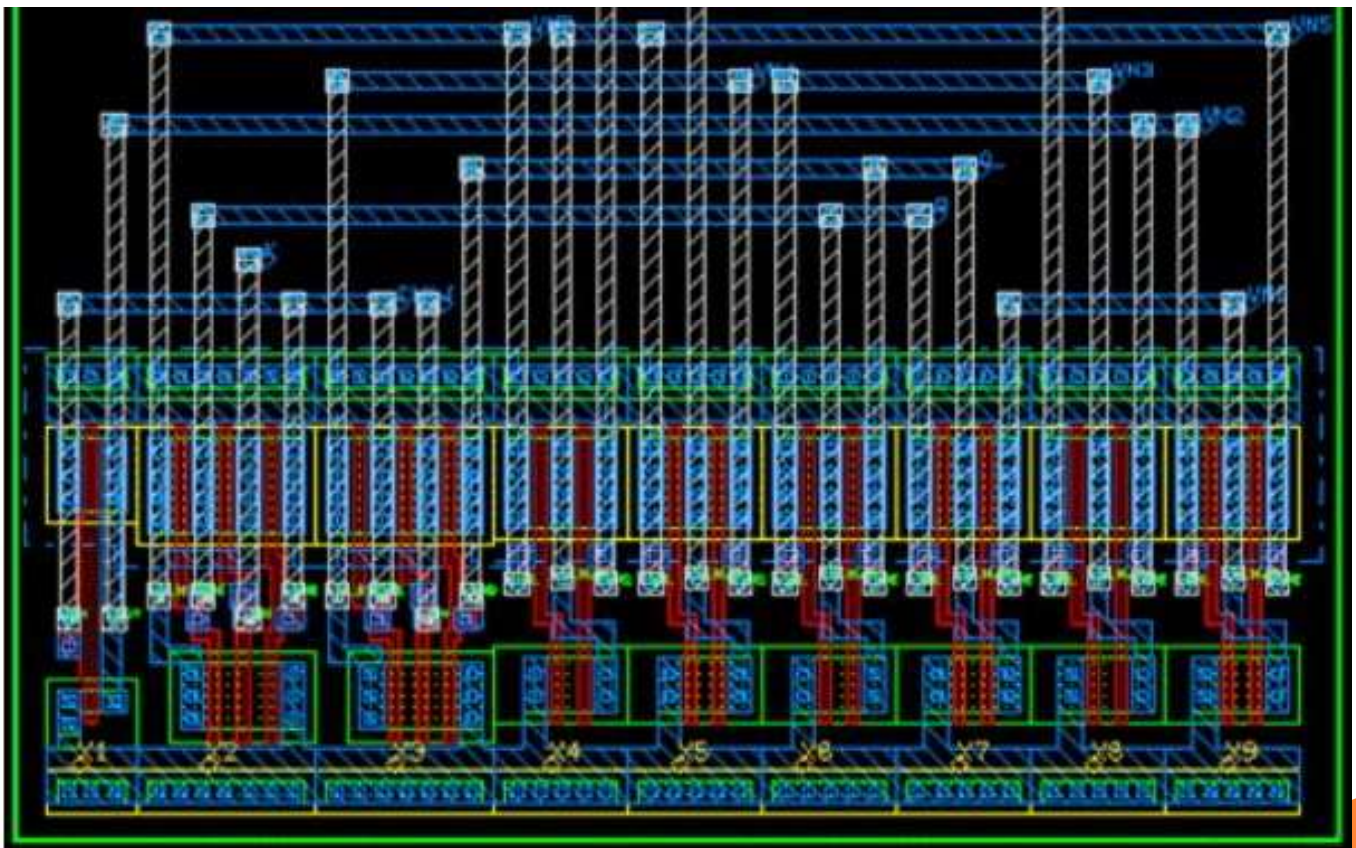


Figure : J-K Flip-Flop