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Empowering Communities...*

Synthesis and Optimization

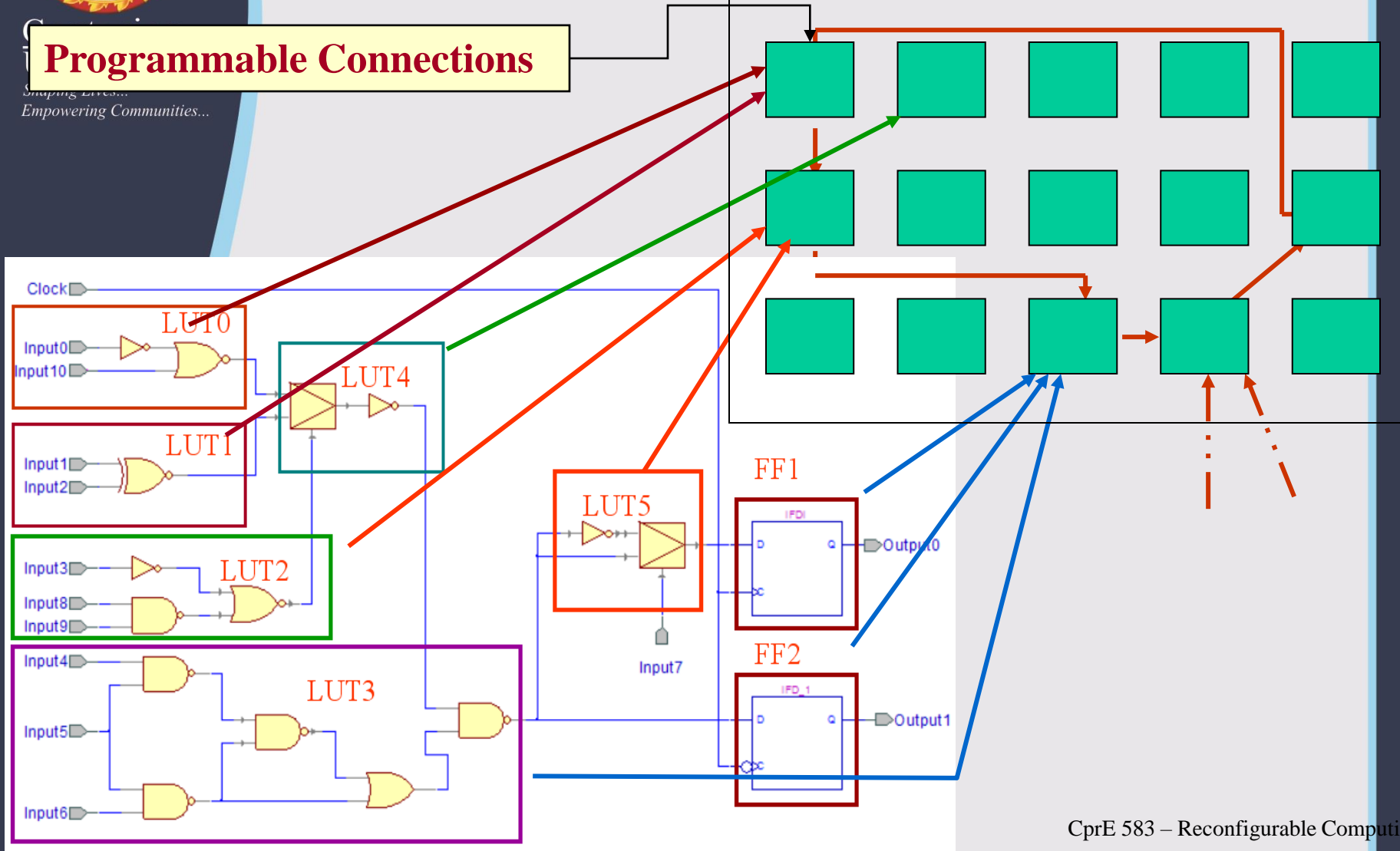


Placing and Routing

FPGA

Programmable Connections

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Timing Score: 0

Place and Route Report

Asterisk (*) preceding a constraint indicates it was not met.

This may be due to a setup or hold violation.

Constraint	Requested	Actual	Logic Levels
TS_clk = PERIOD TIMEGRP "clk" 11.765 ns HIGH 50%	11.765ns	11.622ns	13
OFFSET = OUT 11.765 ns AFTER COMP "clk"	11.765ns	11.491ns	1
OFFSET = IN 11.765 ns BEFORE COMP "clk"	11.765ns	11.442ns	2



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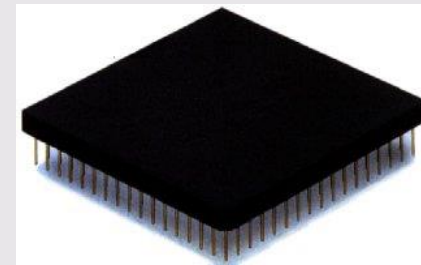
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Configuration

Once a design is implemented, you must create a file that the FPGA can understand

This file is called a bit stream: a BIT file (.bit extension)

The BIT file can be downloaded directly to the FPGA, or can be converted into a PROM file which stores the programming information





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Even when you don't see...*

Logic Synthesis

Syntax-based translation

Translate HDL into logic directly ($ab + ac$)

Generally requires optimization

Macros

Pre-designed logic

Generally identified by language features

Hard macro: includes placement

Soft macro: no placement



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Logic Synthesis Phases

Technology-independent optimizations

Works on Boolean expression equivalent

Estimates size based on number of literals

Uses factorization, resubstitution, minimization to optimize logic

Technology-independent phase uses simple delay models

Technology-dependent optimizations

Maps Boolean expressions into a particular cell library

Mapping may take into account area, delay

Allows more accurate delay models

Transformation from technology-independent to technology-dependent is called **library binding**



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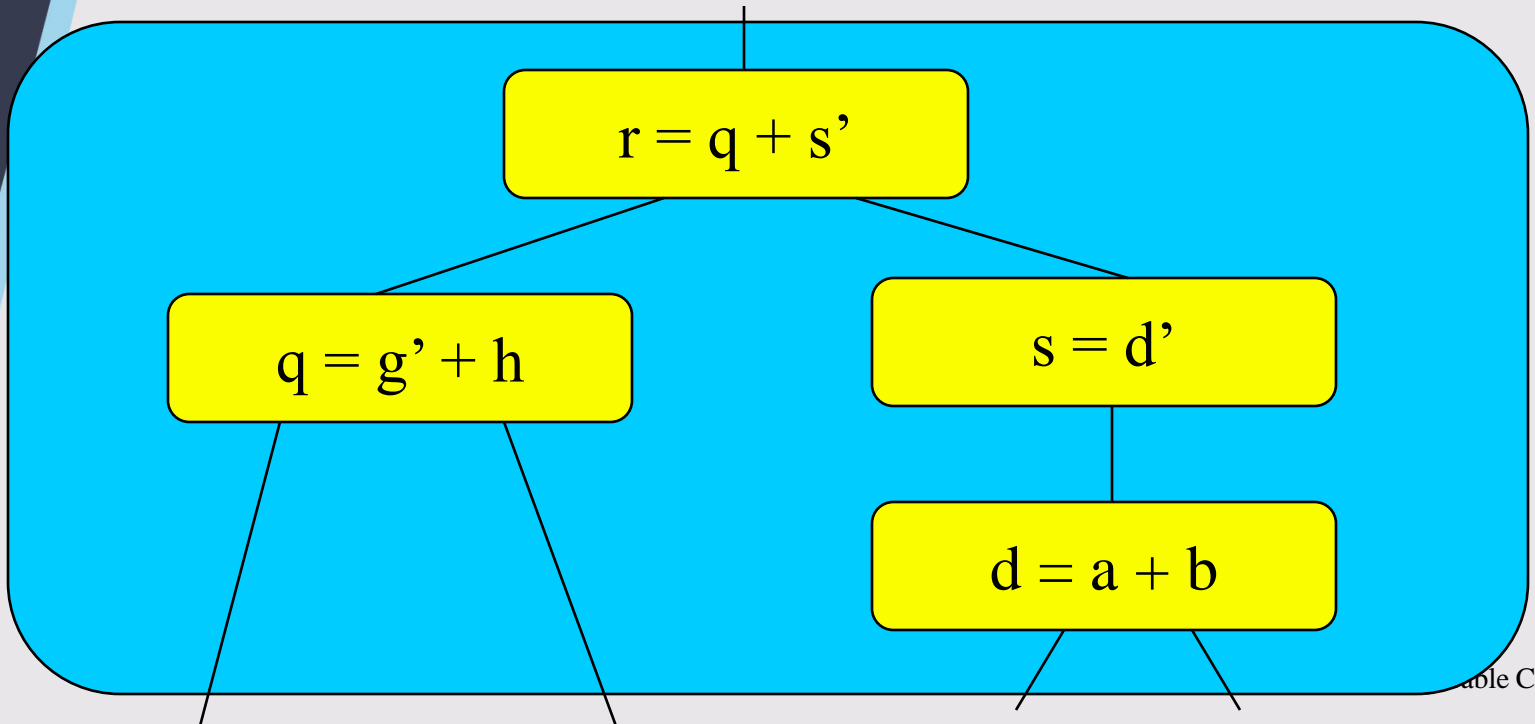
LUT-based Logic Synthesis

Cost metric for static gates is literal

$ax + bx'$ has four literals, requires 8 transistors

Cost metric for FPGAs is logic element

All functions that fit in an LE have the same cost





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Behavioral Synthesis

Sequential operation is not the most abstract description of behavior

We can describe behavior without assigning operations to particular clock cycles

High-level synthesis (behavioral synthesis) transforms an unscheduled behavior into a register-transfer behavior



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Tasks in Behavioral Synthesis

Scheduling – determines clock cycle on which each operation will occur

Allocation – chooses which function units will execute which operations

Data dependencies describe relationships between operations:

$x \leq a + b$; value of x depends on a, b

High-level synthesis must preserve data dependencies