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Clock Domain



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Timing Hazard

Static hazard: possibility of a brief signal value change when the signal was expected to be stable, due to timing (glitch)

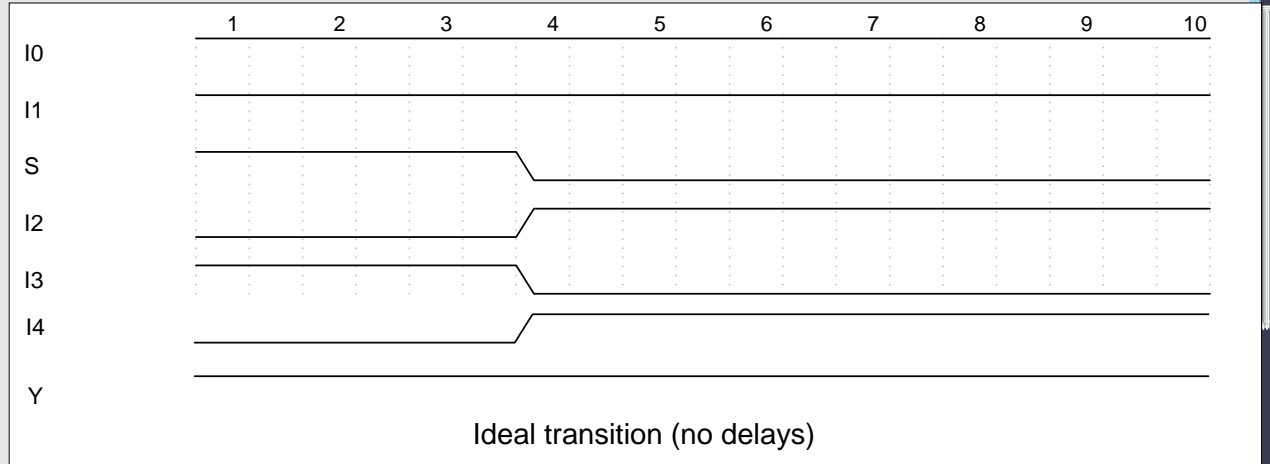
Dynamic hazard: possibility of multiple output transitions caused by a single input transition due to multiple signal paths with different delays



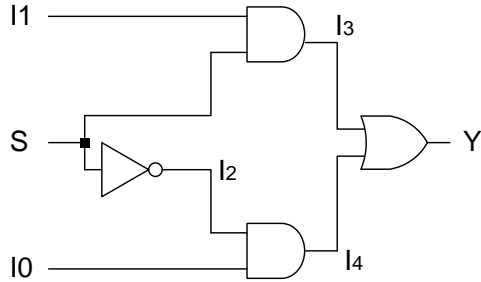
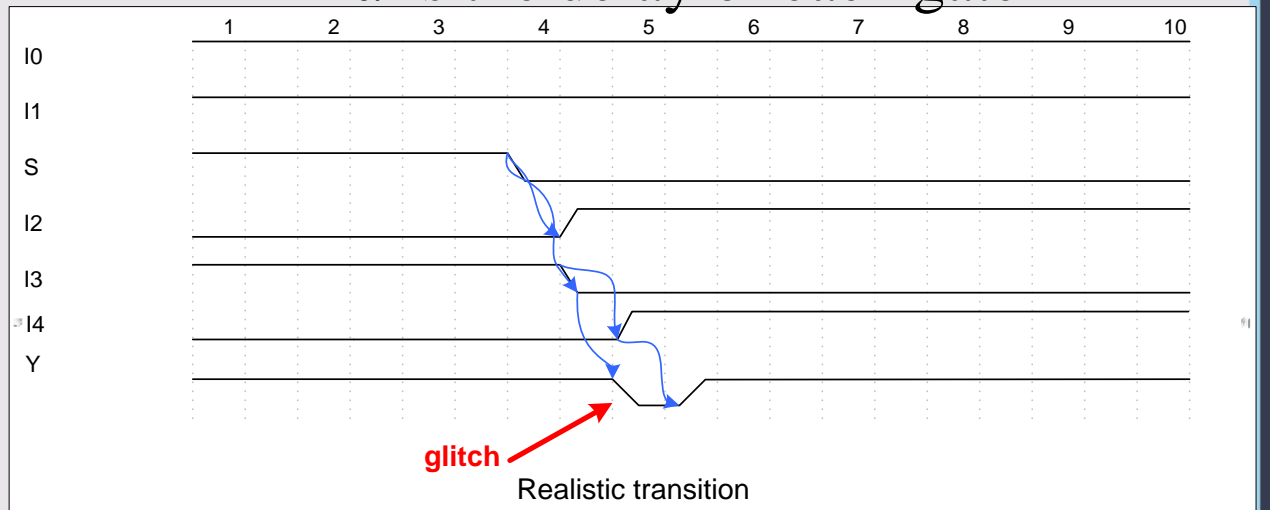
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Static Hazard



If d is the delay of each gate



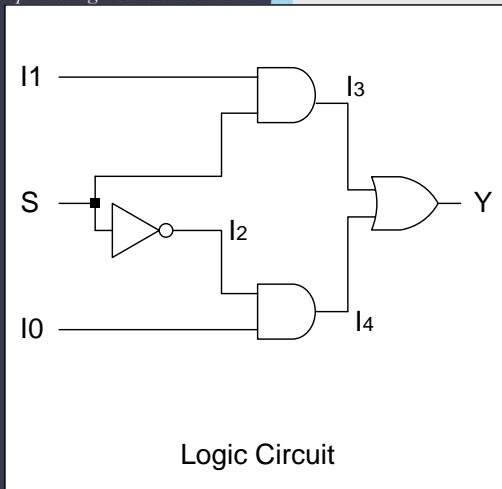
Logic Circuit



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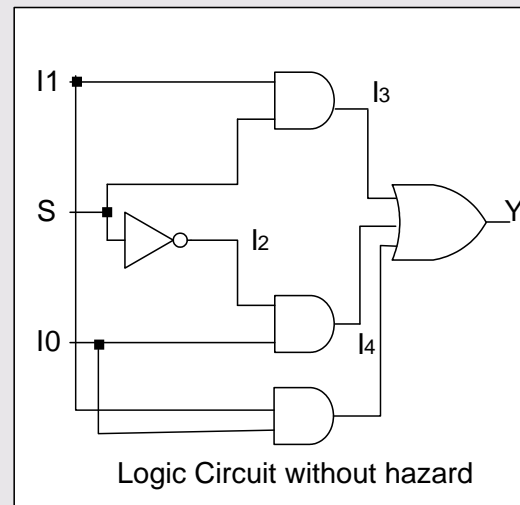
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Analyzing Static Hazards using Karnaugh maps



		I1I0	00	01	11	10
S	0	0	1	1	0	
1	0	0	1	1	0	

		I1I0	00	01	11	10
S	0	0	1	1	0	
1	0	0	1	1	0	



A static hazard can occur when changing a single input variable causes a jump from one prime implicant to another

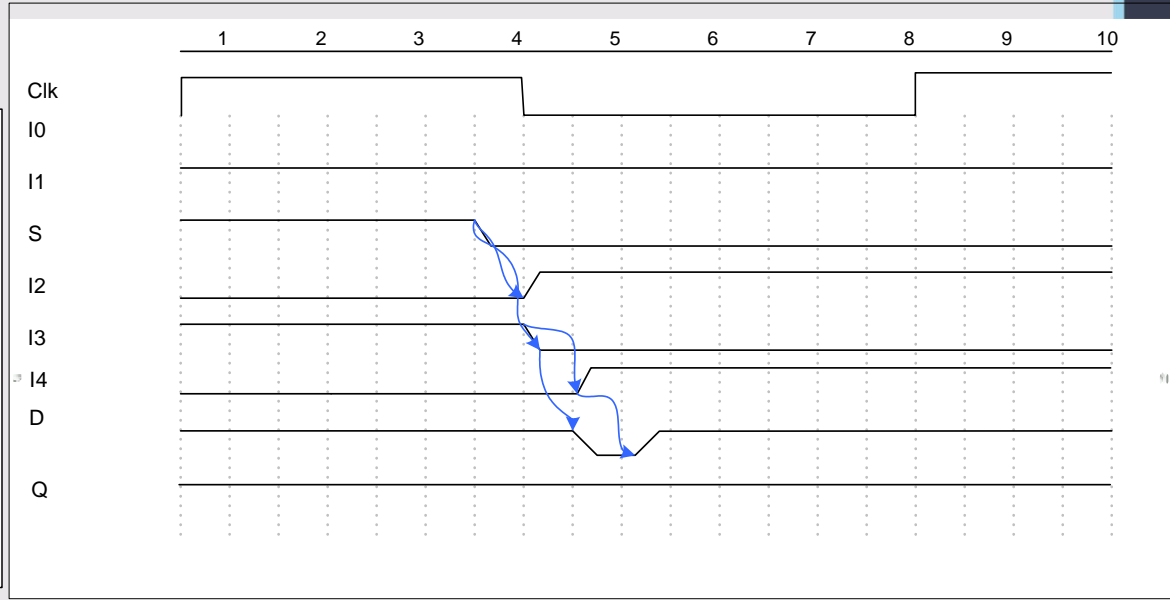
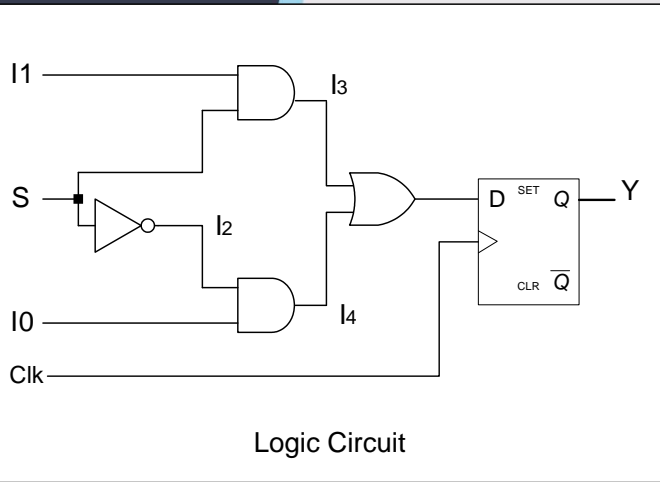
Solution: include an additional prime implicant



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Eliminating hazards using Flip-Flops





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Synchronous Design

Three things must be ensured by the designer:

Minimize and determine clock skew

Account for flip-flop setup and hold times

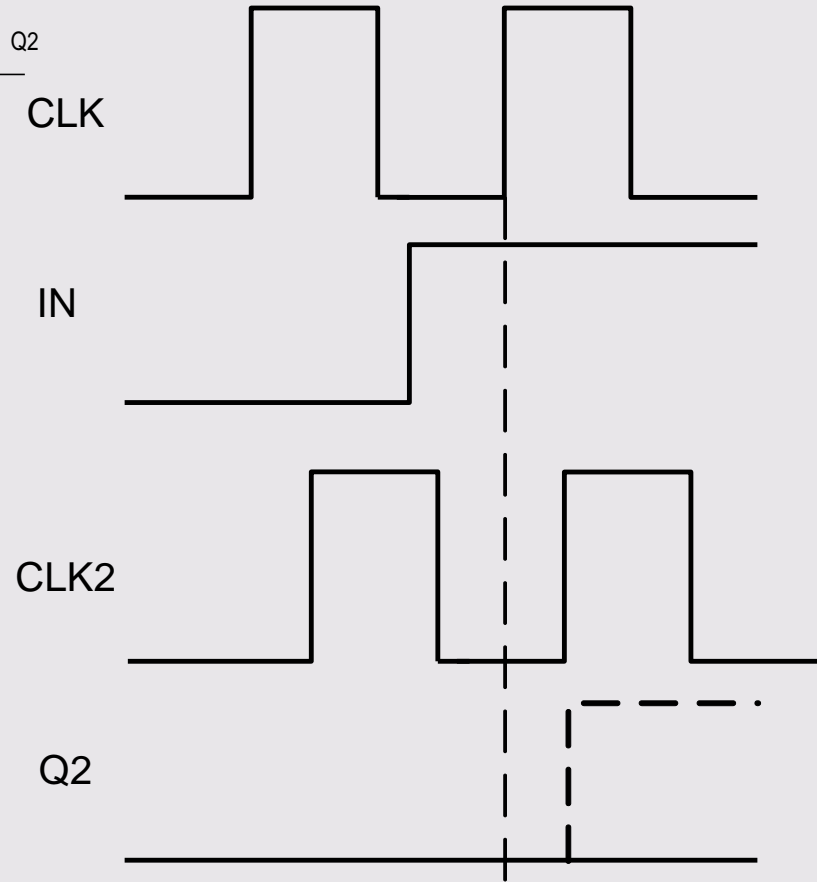
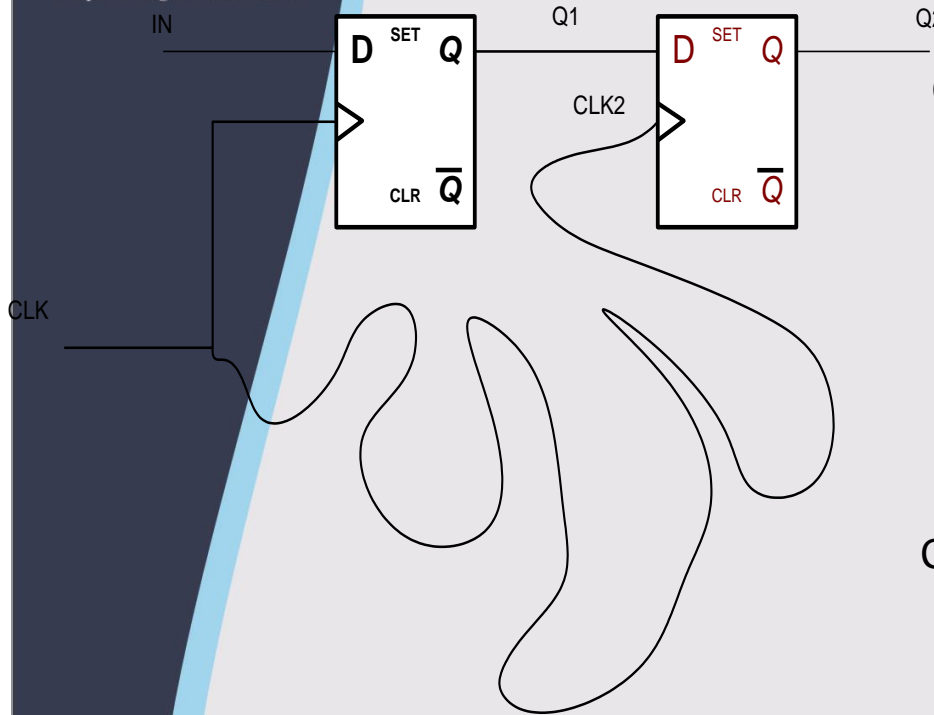
Reliably synchronize asynchronous inputs



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Clock skew



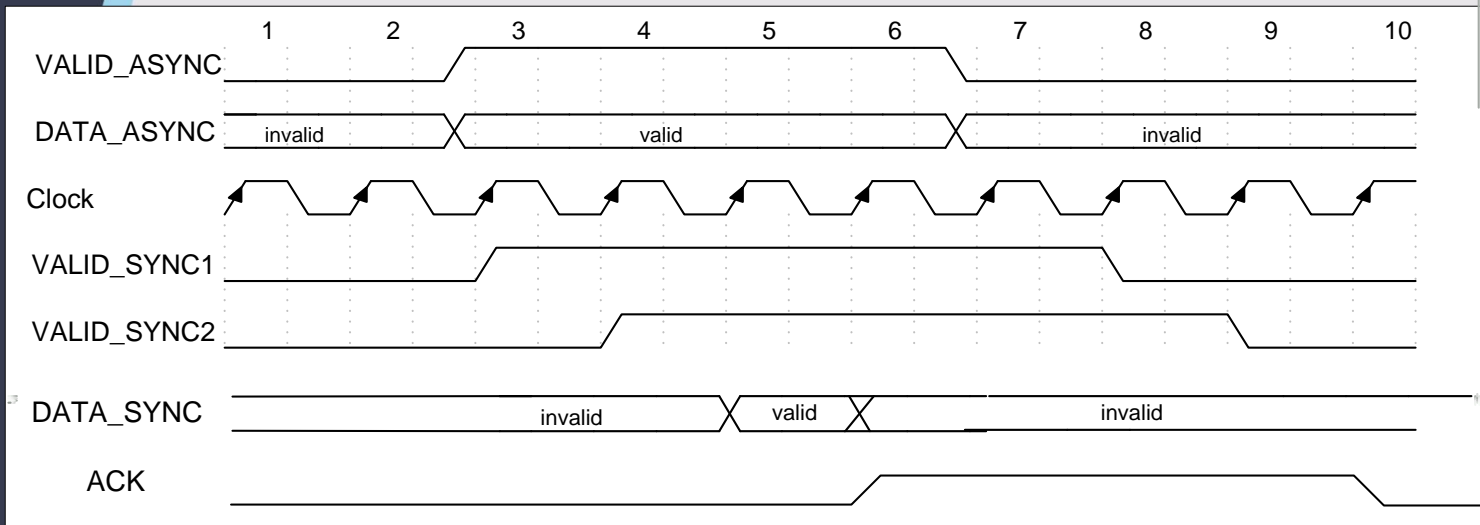
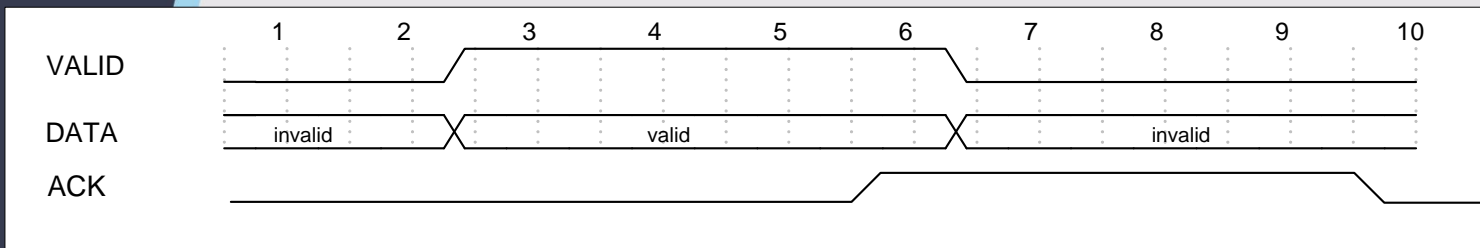
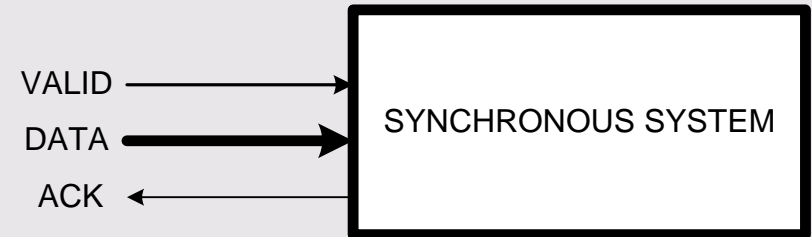


Synchronizing bus transfers

Do **not** use dual f/f synchronizers in all bits, this will only increase the chances of metastability

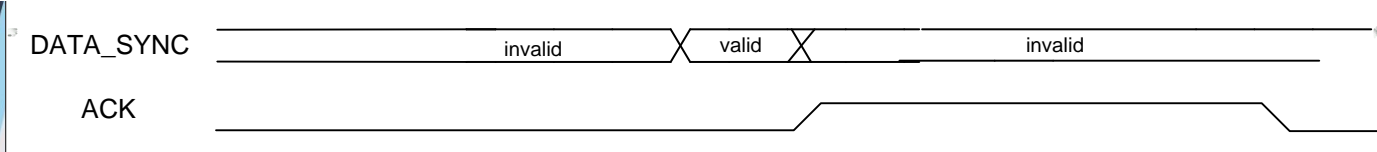
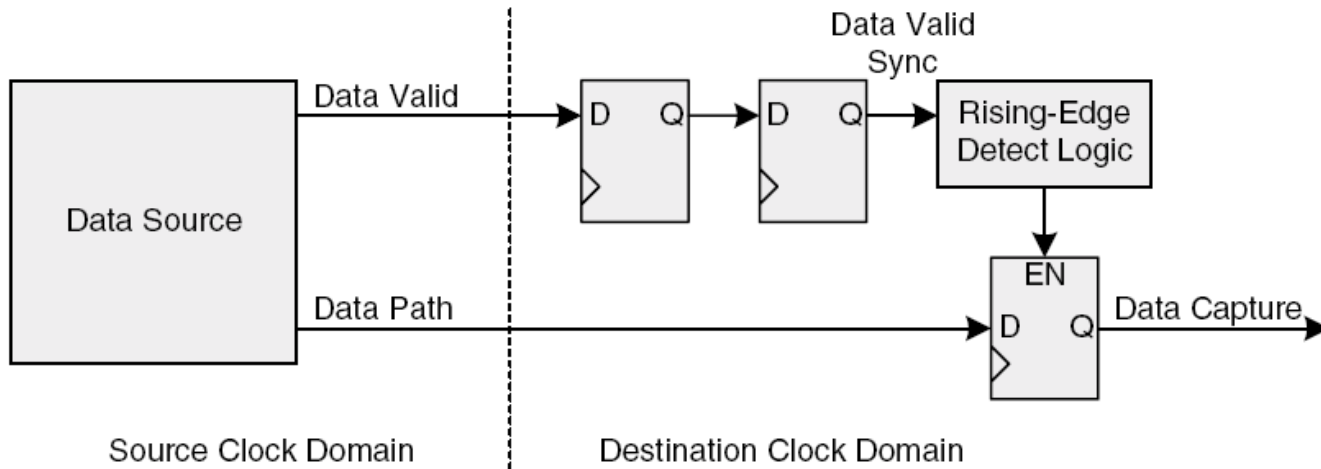
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Synchronize the control signals and read the input when safe to do so





Synchronization circuit



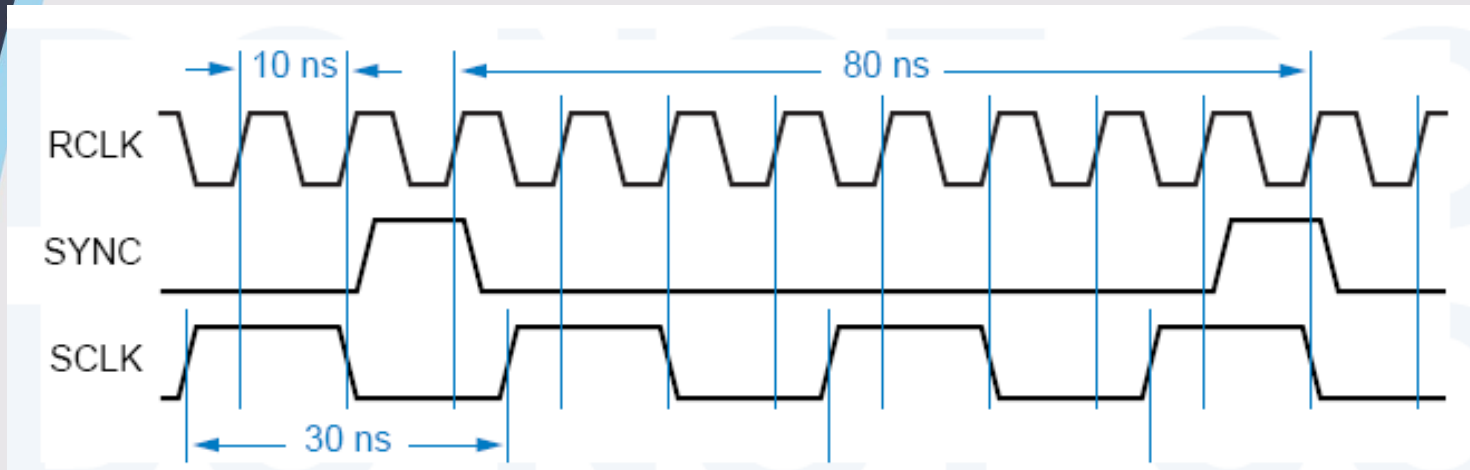


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Synchronizing high-speed data transfers

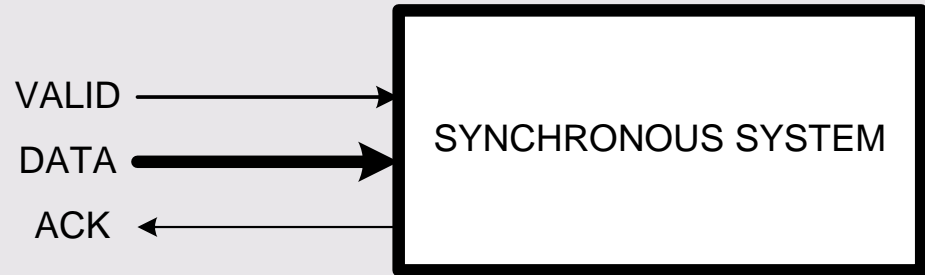
What happens when the asynchronous inputs are clocked faster than the system clock? Or in a long burst transfer such as AXI bus?





FIFO Synchronizer basic concept

On burst transfers, the receiver cannot afford to wait for the signal to settle.



Solution: A dual-port RAM FIFO

Problem: How do we synchronize the counters?

