Centurion
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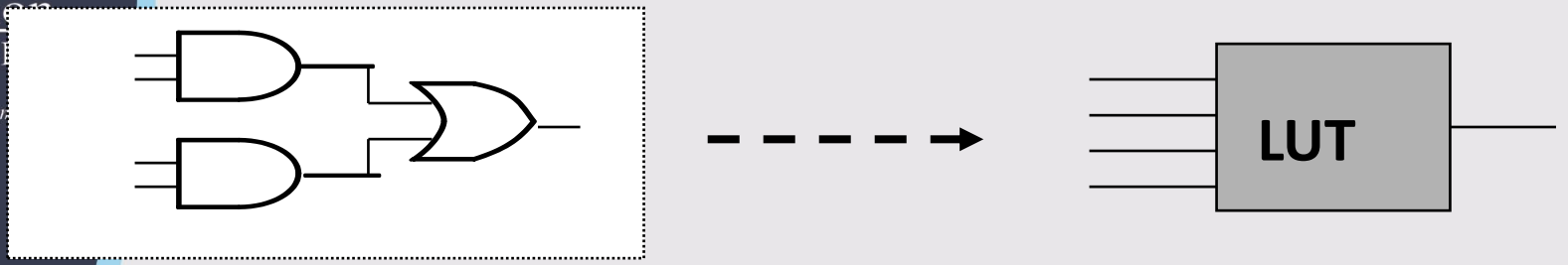
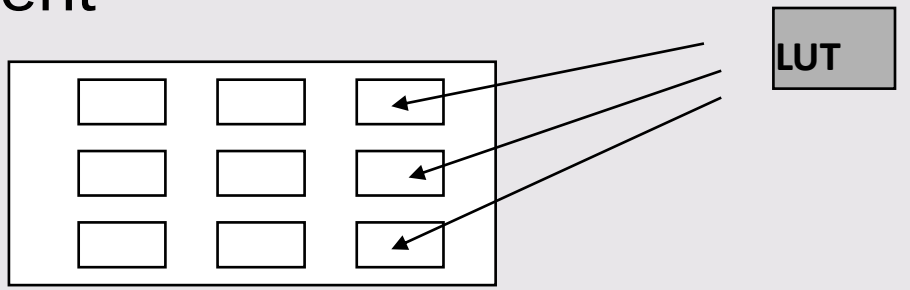
RTL CODING AND SYNTHESIS

FPGA Circuit Compilation

- Technology Mapping

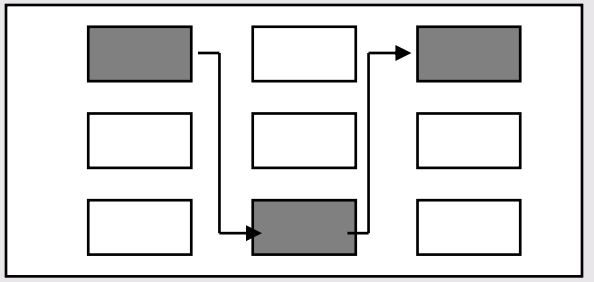


- Placement



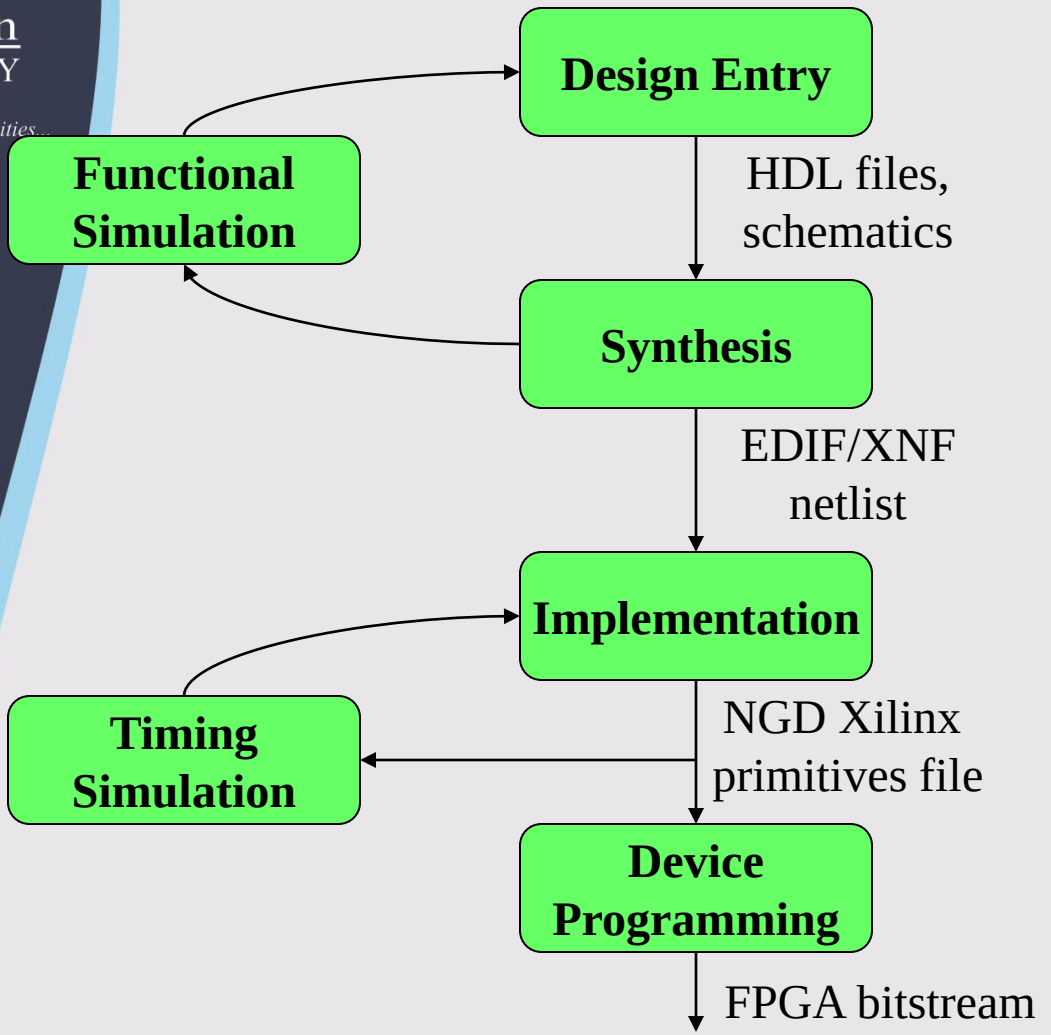
Assign a logical LUT to a physical location

- Routing



Select wire segments and switches for interconnection

FPGA Design Flow (Xilinx)



Design Flow with Test

Design and implement a simple unit permitting to speed up encryption with RC5-similar cipher with fixed key set on 8031 microcontroller. Unlike in the experiment 5, this time your unit has to be able to perform an encryption algorithm by itself, executing 32 rounds…..

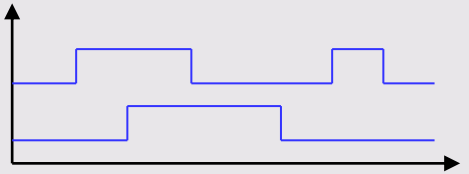
Specification

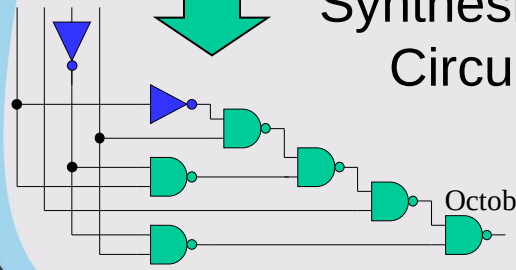
```
Library IEEE;
use ieee.std_logic_1164.all;
use ieee.std_logic_unsigned.all;

entity RC5_core is
        port(
                clock, reset, encr_decr: in std_logic;
                data_input: in std_logic_vector(31 downto 0);
                data_output: out std_logic_vector(31 downto 0);
                out_full: in std_logic;
                key_input: in std_logic_vector(31 downto 0);
                key_read: out std_logic;
        );
end RC5_core;
```

VHDL description

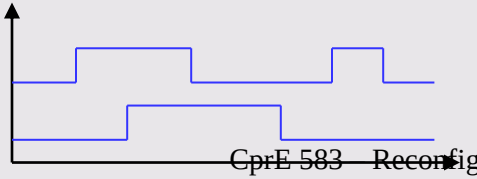
Functional simulation





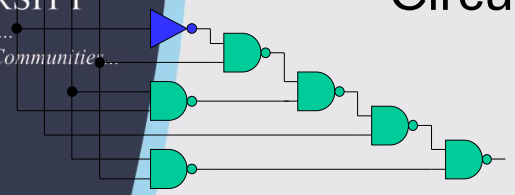
Synthesized Circuit

Post-synthesis simulation

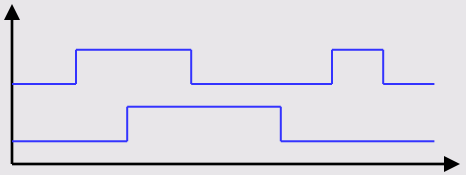


Design Flow with Test (cont.)

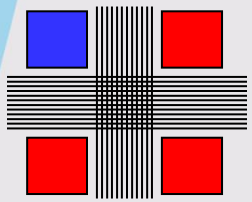
Synthesized Circuit



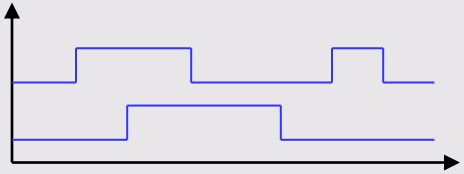
Post-synthesis simulation



Implementation

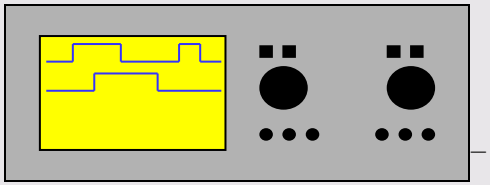


Timing simulation



Configuration

On chip testing



Synthesis Tools

Interpret RTL code

Produce synthesized circuit netlist in a standard EDIF format

Give preliminary performance estimates

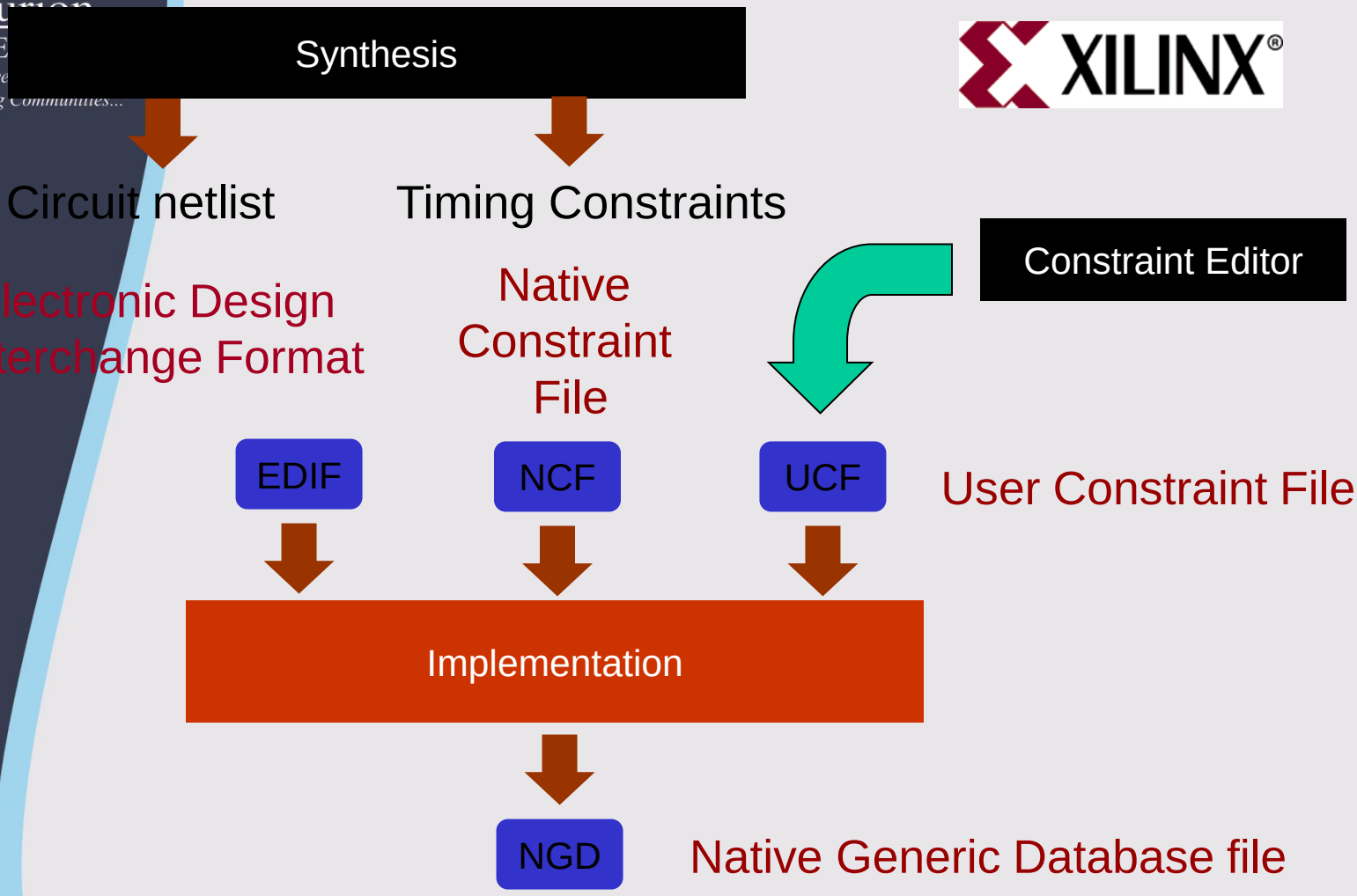
Display circuit schematic corresponding to EDIF netlist

```
Performance Summary
*******************

Worst slack in design: -0.924

                           Requested     Estimated     Requested     Estimated
                               Clock         Clock
Starting Clock     Frequency     Frequency     Period        Period
   Slack      Type                   Group
------------------------------------------------------------------------------
   ----------------------
exam1|clk          85.0 MHz      78.8 MHz      11.765        12.688        -0.924
   inferred     Inferred_clkgroup_0
System             85.0 MHz      86.4 MHz      11.765        11.572        0.193
   system       default_clkgroup
==============================================================================
```

Implementation



Circuit Netlist and Mapping