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Introduction to System Verilog



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What is System Verilog

SystemVerilog is a combined hardware description language and hardware verification language

SystemVerilog is an extensive set of enhancements to IEEE 1364 Verilog-2001 standards

It has features inherited from Verilog HDL, VHDL, C, C++



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History and evolution of SV

Verilog (IEEE standard 1364)

Began in 1983 as a proprietary language

Opened to the public in 1992

Became an IEEE standard in 1995 (updated in 2001 and 2005)

Between 1983 and 2005 design sizes increased dramatically!

System Verilog (IEEE standard 1800)

Originally intended to be the 2005 update to Verilog

Contains hundreds of enhancements and extensions to Verilog

Published in 2005 as a separate document

Officially superseded Verilog in 2009

Updated with more features in 2012 (IEEE 1800 2012 standard)



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System Verilog – User View

Has 5 major parts

SVD – System Verilog for Design

Features supporting Design

SVTB – System Verilog for Test benches

Test bench specific Features

SVA – System Verilog Assertions

Features for temporal and concurrent assertions

SVDPI – SV Direct Programming Interface

For better C/C++ integration

SVAPI – SV Application Programming Interface

For better Coverage/Assertion integration



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System Verilog for Verification

Where do we really use System Verilog Language in Verification ?

Building Test bench components

Reference Models



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Now Let us get into coding !