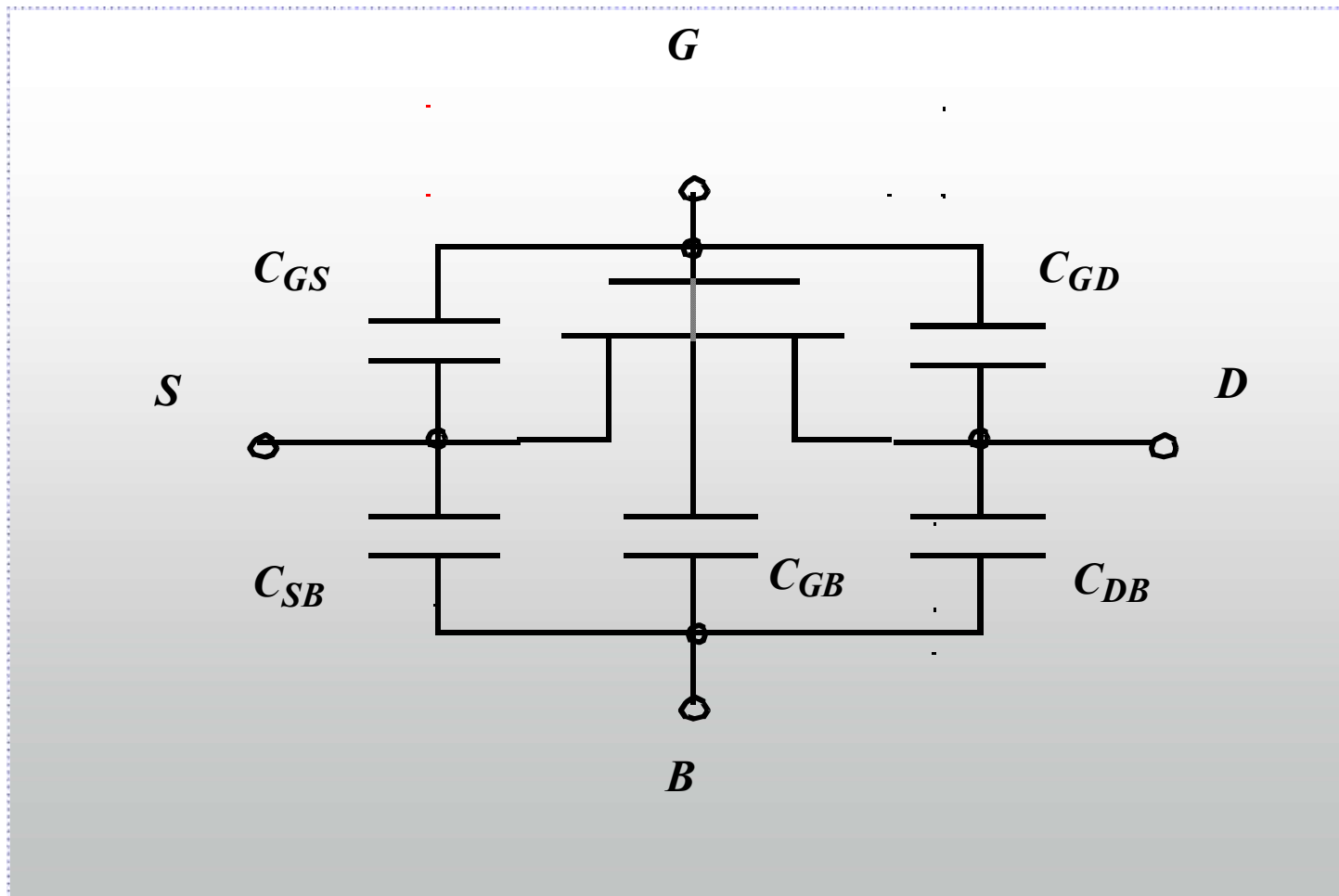


MOS Capacitances

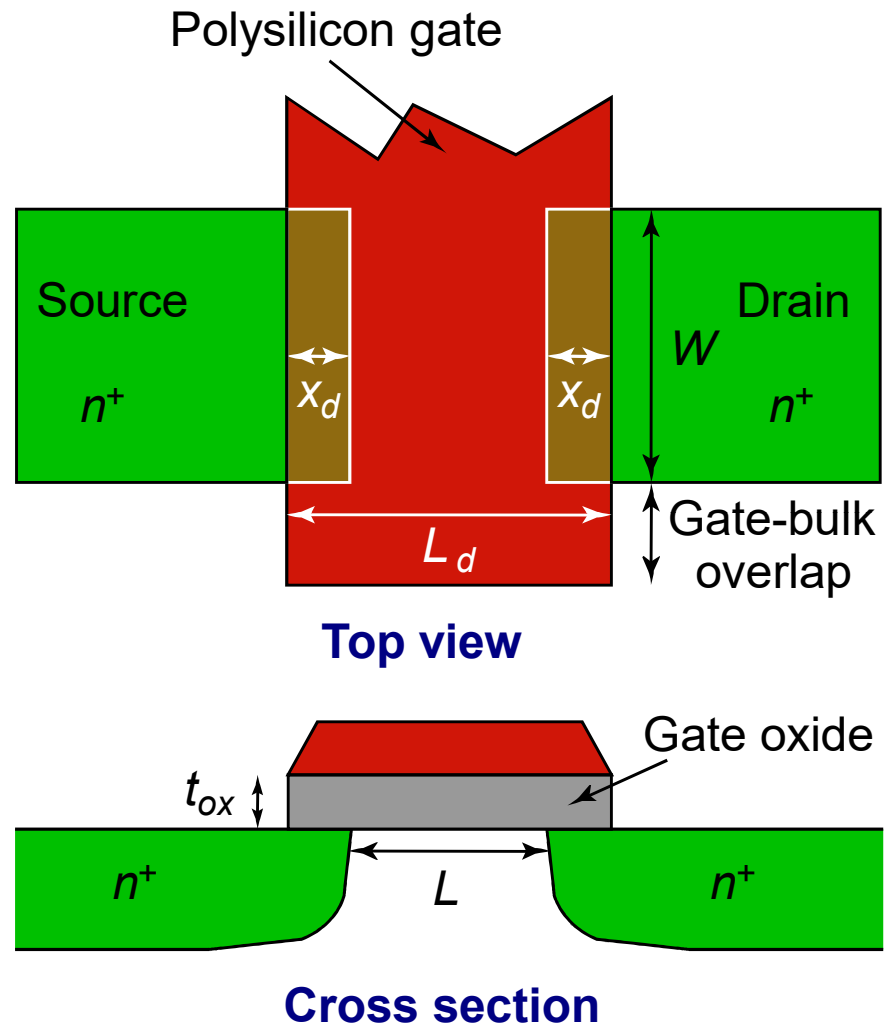
Dynamic Behavior



Dynamic Behavior of MOS Transistor

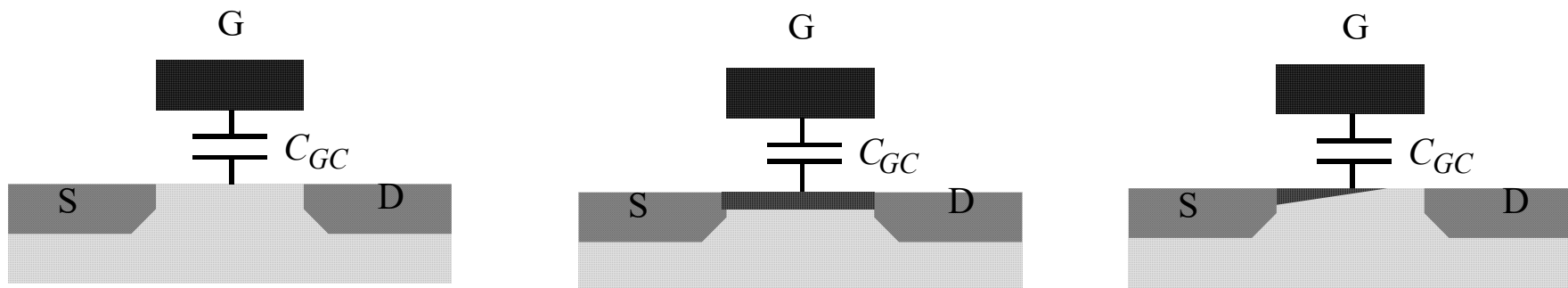


The Gate Capacitance



$$C_{gate} = \frac{\epsilon_{ox}}{t_{ox}} WL$$

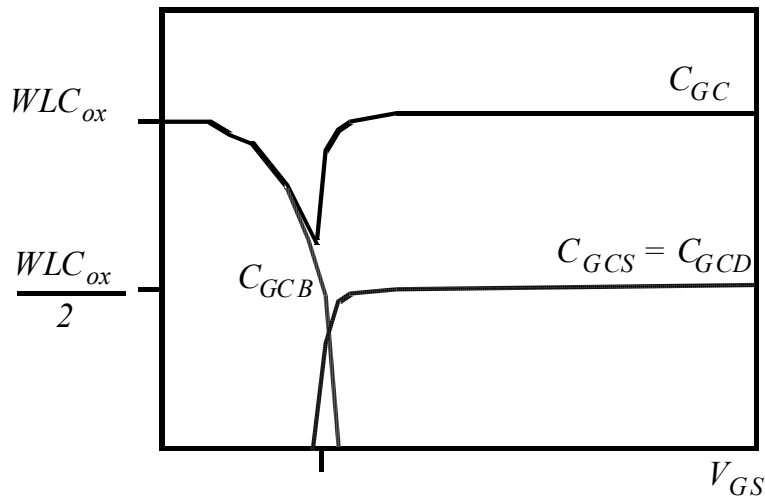
Gate Capacitance



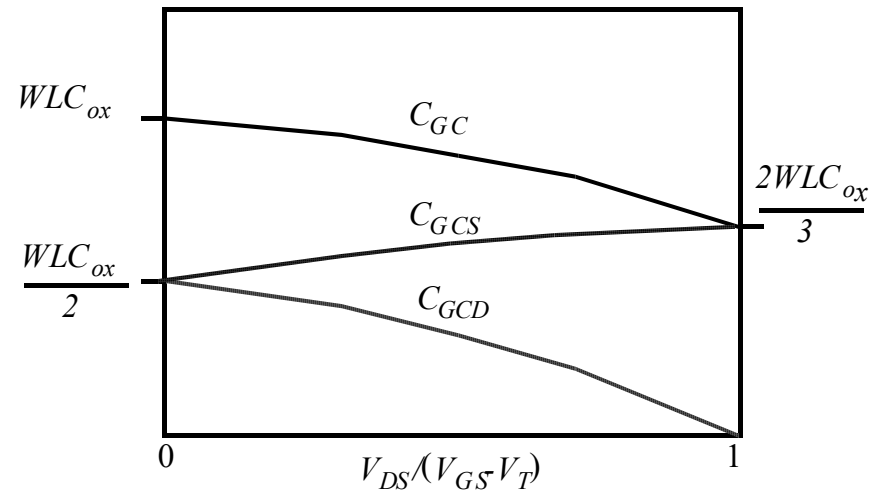
Operation Region	C_{gb}	C_{gs}	C_{gd}
Cutoff	$C_{ox}WL_{eff}$	0	0
Triode	0	$C_{ox}WL_{eff}/2$	$C_{ox}WL_{eff}/2$
Saturation	0	$(2/3)C_{ox}WL_{eff}$	0

Most important regions in digital design: saturation and cut-off

Gate Capacitance

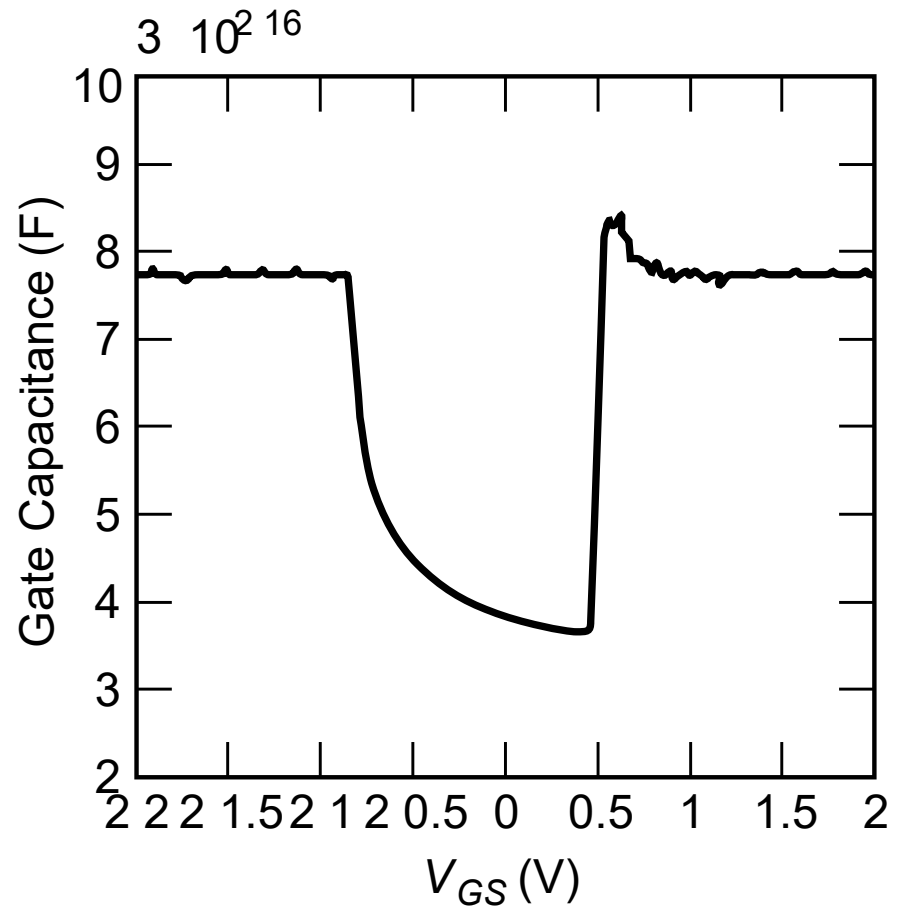
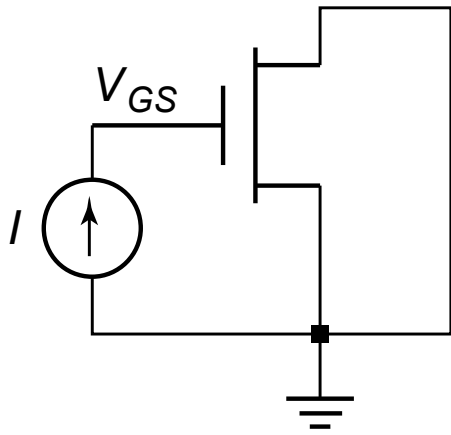


Capacitance as a function of V_{GS}
(with $V_{DS} = 0$)

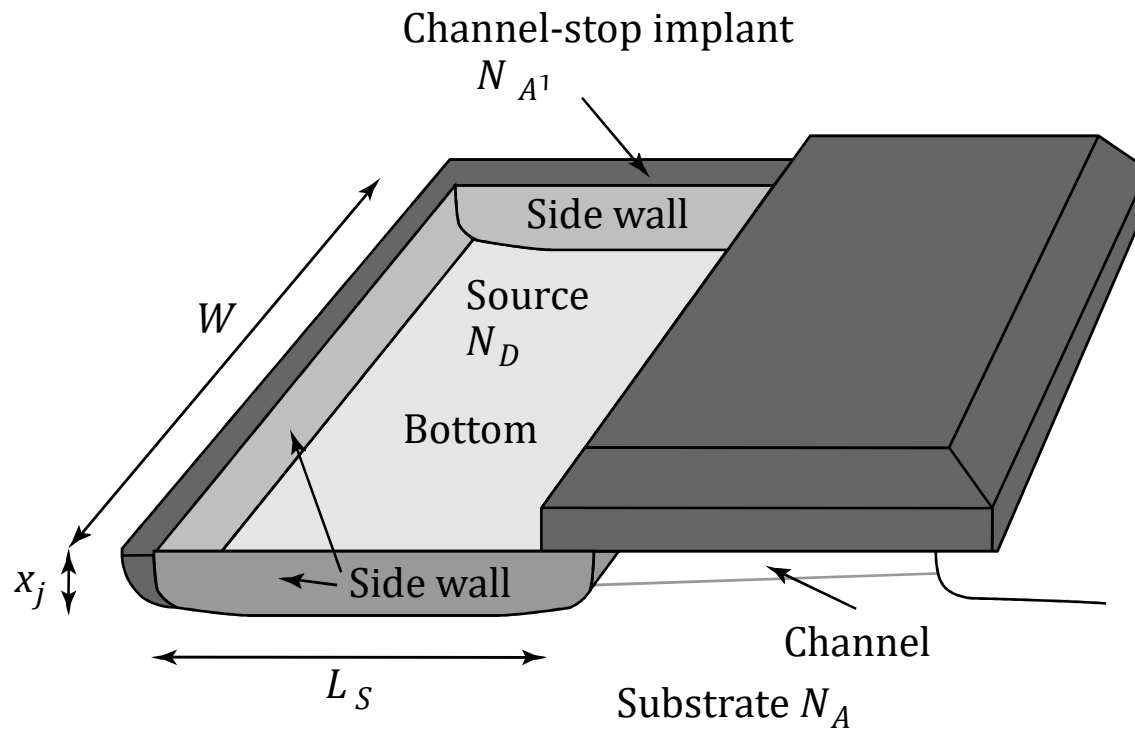


Capacitance as a function of the
degree of saturation

Measuring the Gate Cap

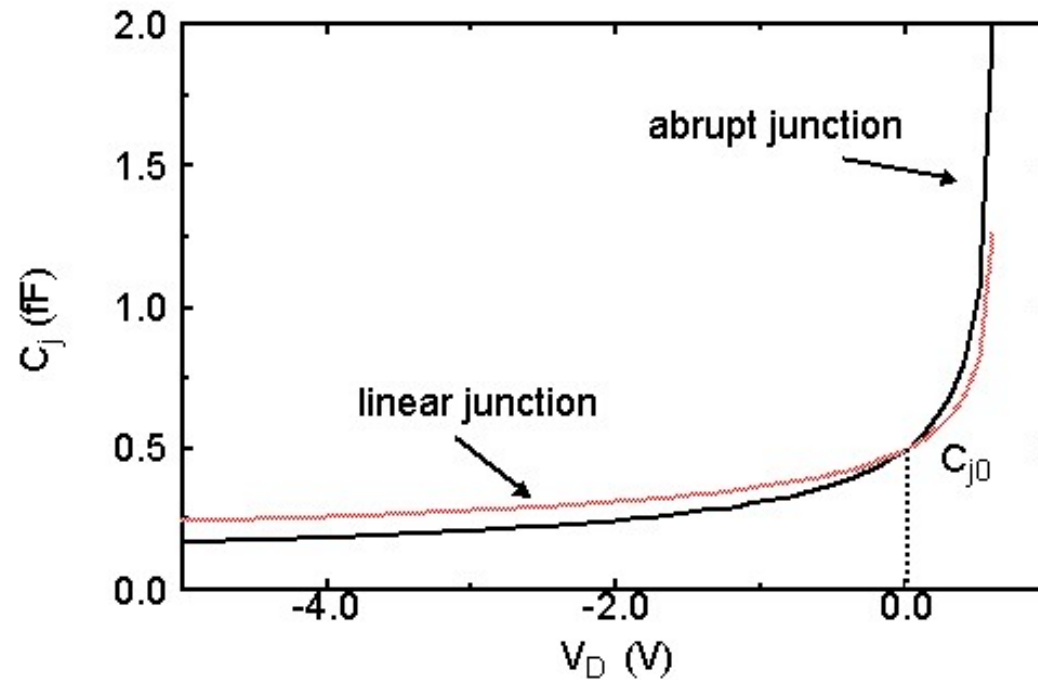


Diffusion Capacitance



$$\begin{aligned} C_{diff} &= C_{bottom} + C_{sw} = C_j \times AREA + C_{jsw} \times PERIMETER \\ &= C_j L_S W + C_{jsw} (2L_S + W) \end{aligned}$$

Junction Capacitance



$$C_j = \frac{C_{j0}}{(1 - V_D / \phi_0)^m}$$

$m = 0.5$: abrupt junction
 $m = 0.33$: linear junction

Linearizing the Junction Capacitance

Replace non-linear capacitance by
large-signal equivalent linear capacitance
which displaces equal charge
over voltage swing of interest

$$C_{eq} = \frac{\Delta Q_j}{\Delta V_D} = \frac{Q_j(V_{high}) - Q_j(V_{low})}{V_{high} - V_{low}} = K_{eq} C_{j0}$$

$$K_{eq} = \frac{-\phi_0^m}{(V_{high} - V_{low})(1 - m)} [(\phi_0 - V_{high})^{1-m} - (\phi_0 - V_{low})^{1-m}]$$

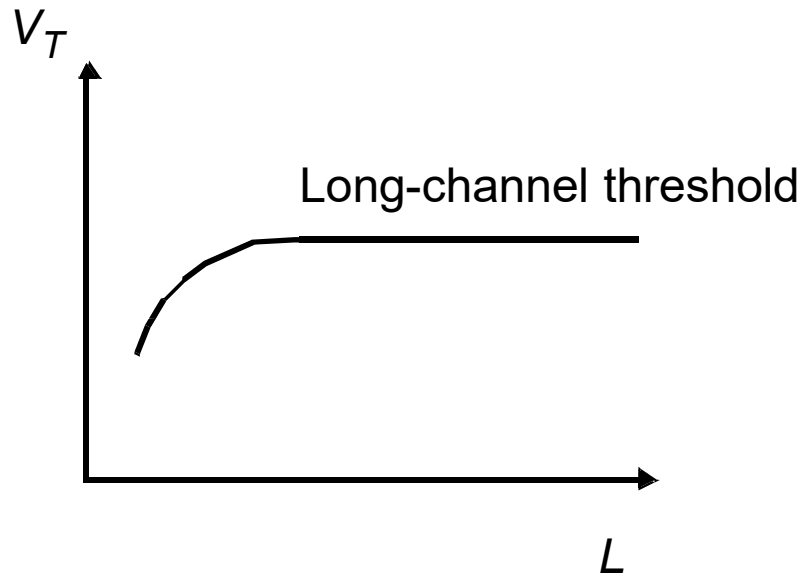
Capacitances in 0.25 μm CMOS process

	C_{ox} (fF/ μm^2)	C_{o} (fF/ μm)	C_{j} (fF/ μm^2)	m_{j}	ϕ_{b} (V)	C_{jsw} (fF/ μm)	m_{jsw}	ϕ_{bsw} (V)
NMOS	6	0.31	2	0.5	0.9	0.28	0.44	0.9
PMOS	6	0.27	1.9	0.48	0.9	0.22	0.32	0.9

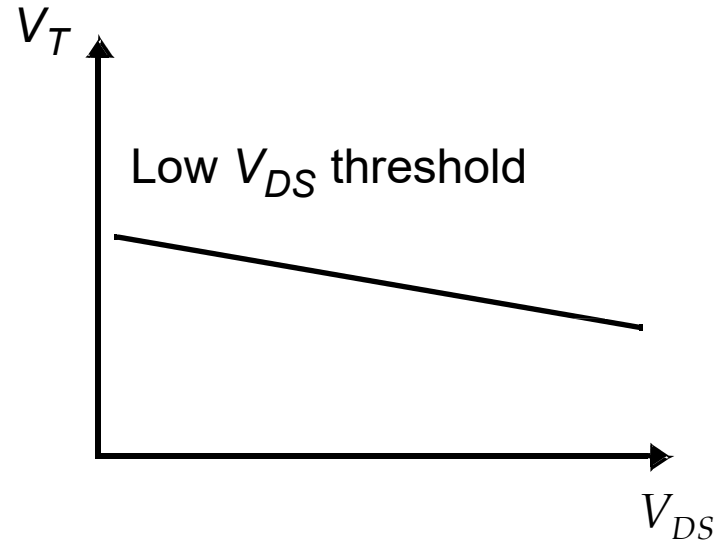
The Sub-Micron MOS Transistor

- ❑ **Threshold Variations**
- ❑ **Subthreshold Conduction**
- ❑ **Parasitic Resistances**

Threshold Variations

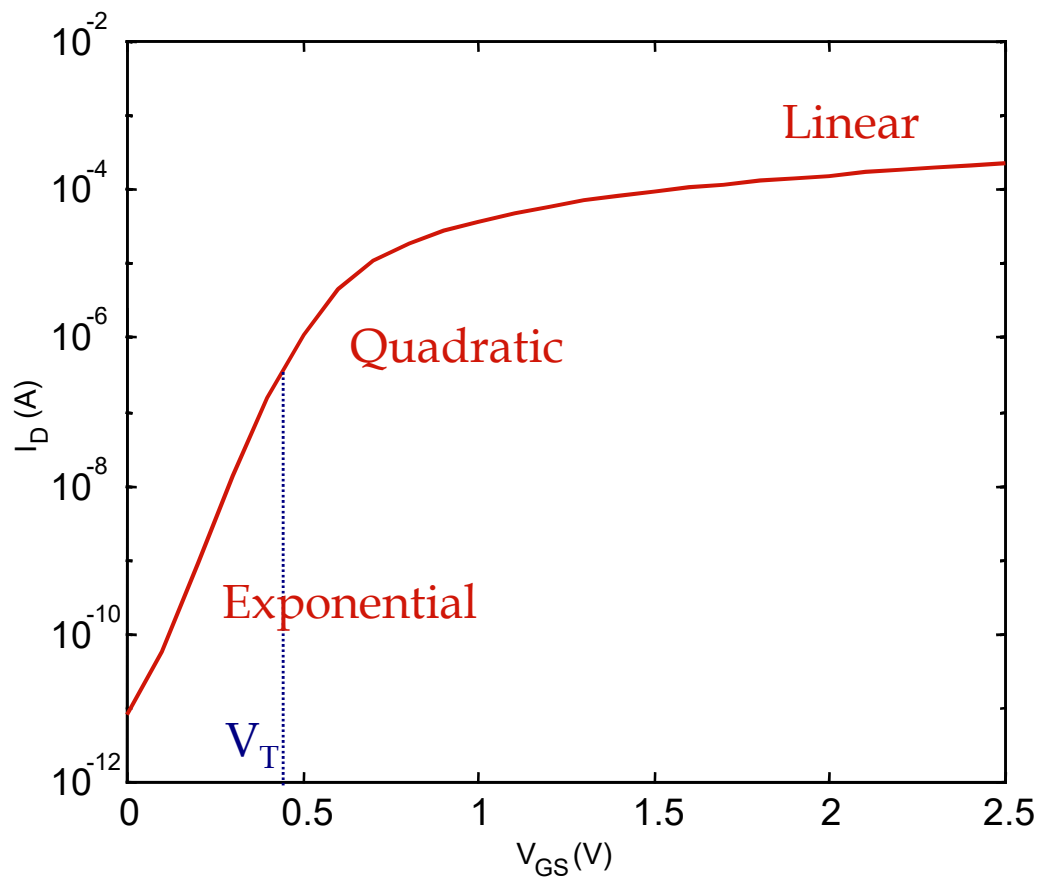


Threshold as a function of the length (for low V_{DS})



Drain-induced barrier lowering (for low L)

Sub-Threshold Conduction



The Slope Factor

$$I_D \sim I_0 e^{\frac{qV_{GS}}{nkT}}, \quad n = 1 + \frac{C_D}{C_{ox}}$$

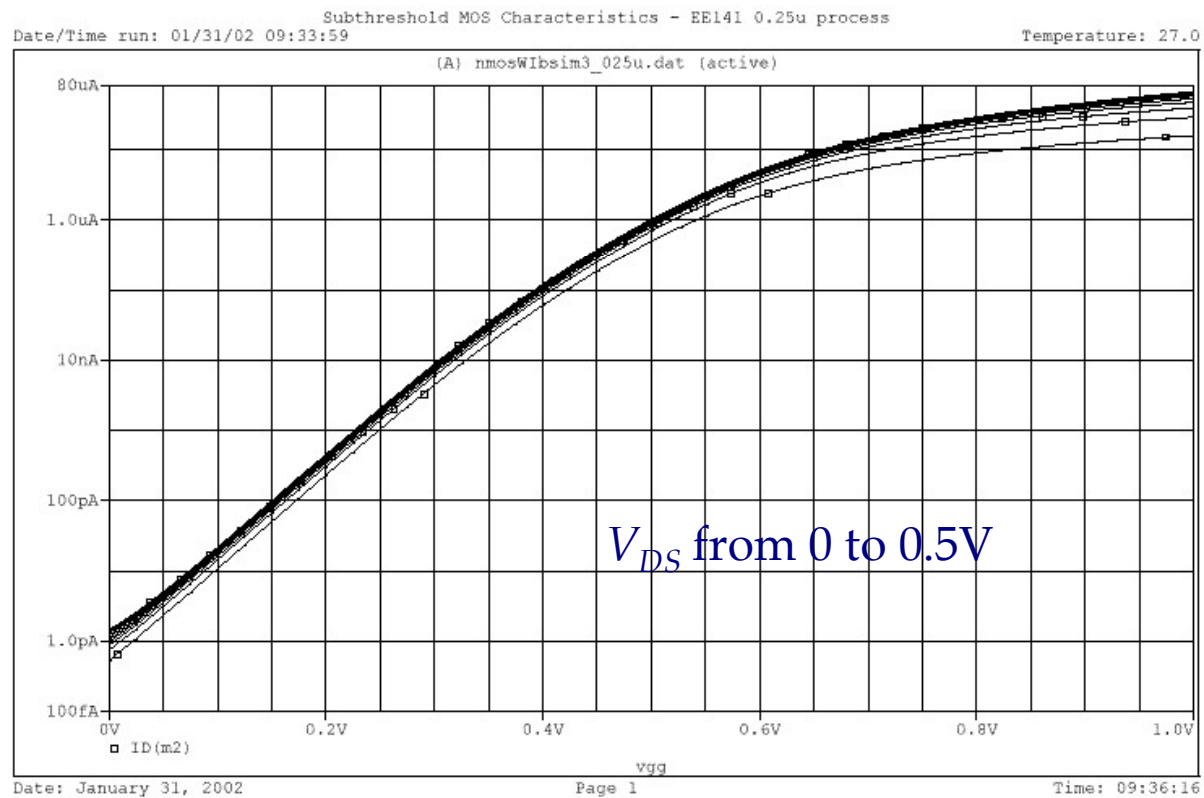
S is ΔV_{GS} for $I_{D2}/I_{D1} = 10$

$$S = n \left(\frac{kT}{q} \right) \ln(10)$$

Typical values for S :
60 .. 100 mV/decade

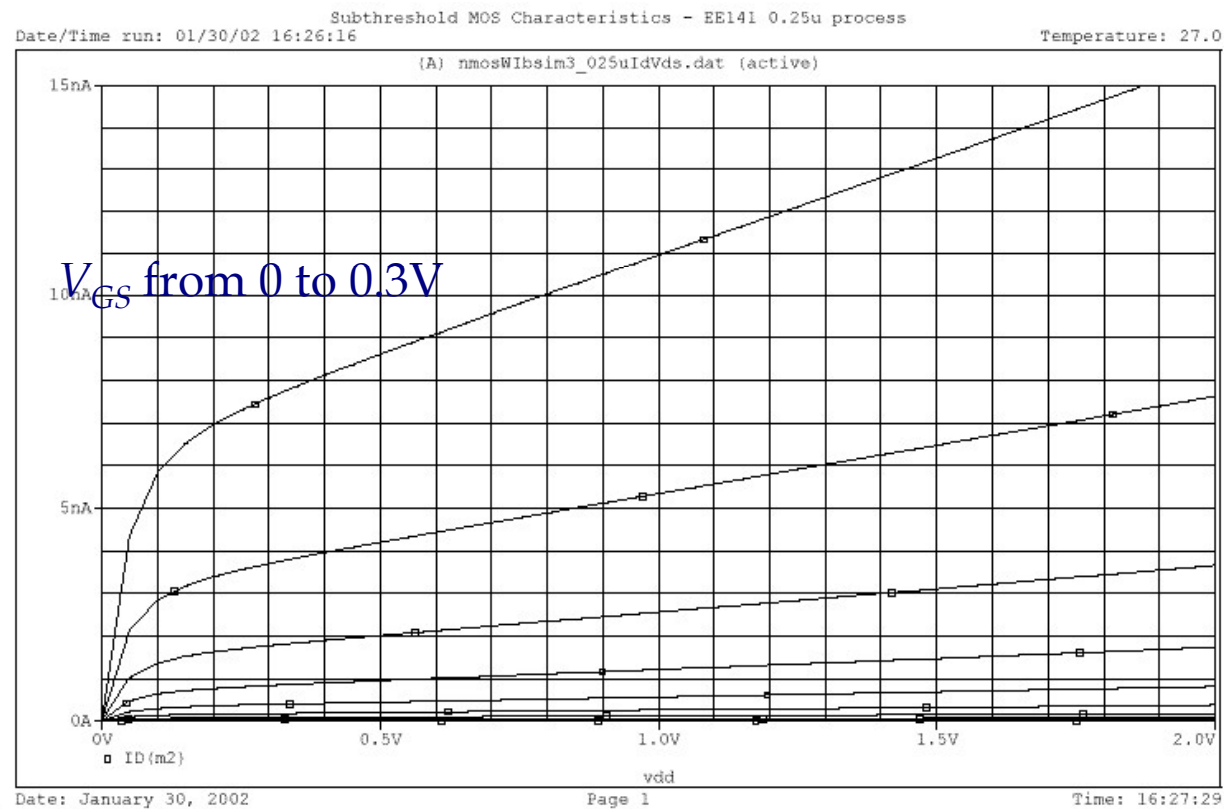
Sub-Threshold I_D vs V_{GS}

$$I_D = I_0 e^{\frac{qV_{GS}}{nkT}} \left(1 - e^{-\frac{qV_{DS}}{kT}} \right)$$



Sub-Threshold I_D vs V_{DS}

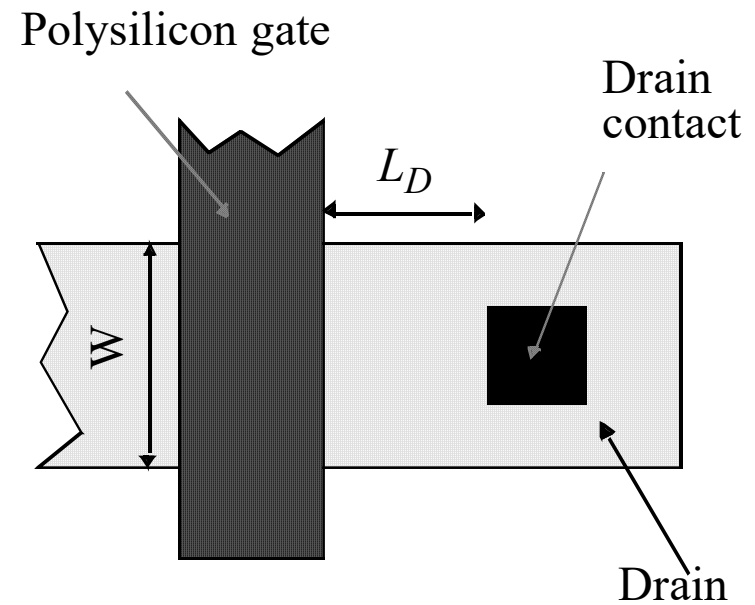
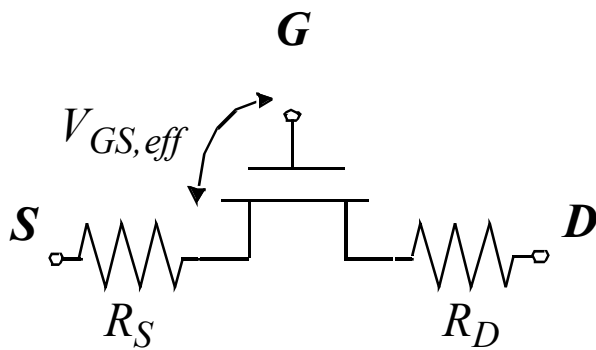
$$I_D = I_0 e^{\frac{qV_{GS}}{nkT}} \left(1 - e^{-\frac{qV_{DS}}{kT}} \right) (1 + \lambda \cdot V_{DS})$$



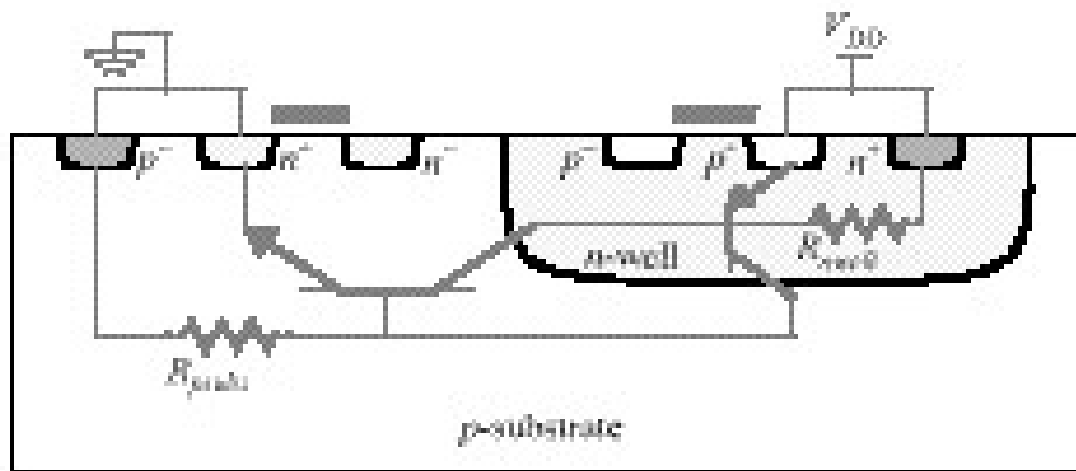
Summary of MOSFET Operating Regions

- Strong Inversion $V_{GS} > V_T$
 - Linear (Resistive) $V_{DS} < V_{DSAT}$
 - Saturated (Constant Current) $V_{DS} \geq V_{DSAT}$
- Weak Inversion (Sub-Threshold) $V_{GS} \leq V_T$
 - Exponential in V_{GS} with linear V_{DS} dependence

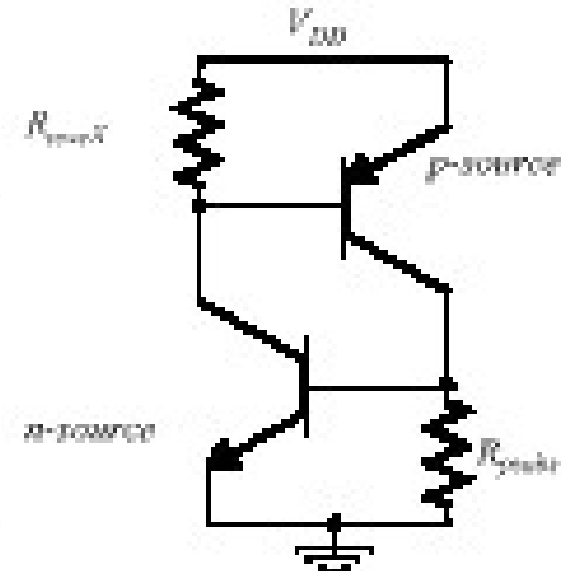
Parasitic Resistances



Latch-up

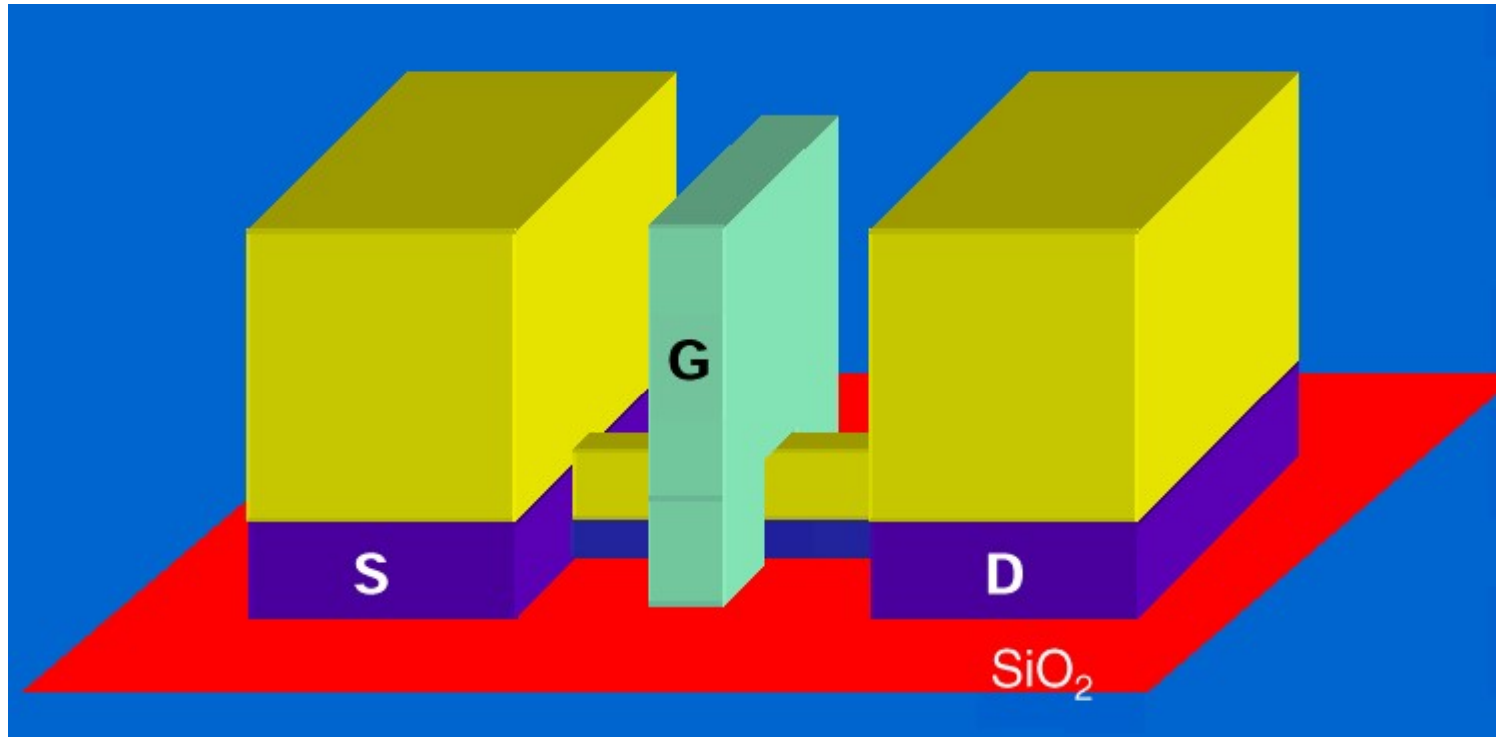


(a) Origin of latchup



(b) Equivalent circuit

Future Perspectives



25 nm FINFET MOS transistor