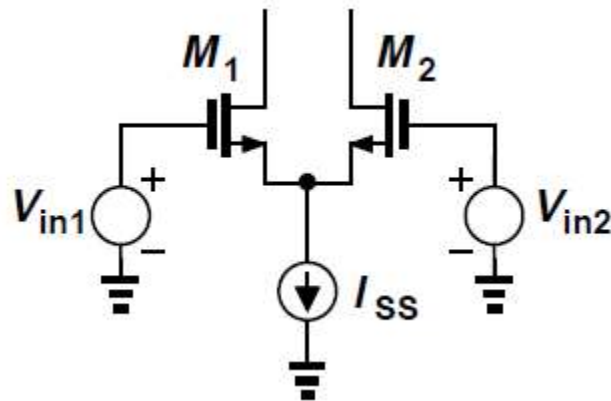


# Half-Circuit Technique

- The half-circuit technique can be applied even if the two inputs are not fully differential

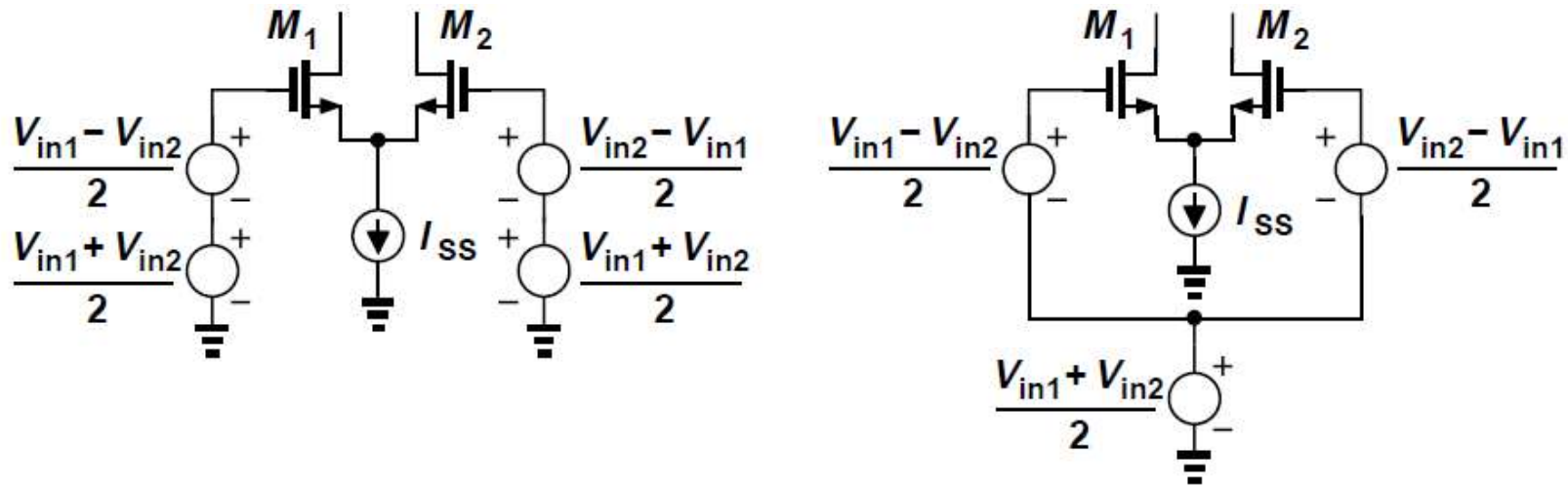


- The unsymmetrical inputs  $V_{in1}$  and  $V_{in2}$  each can be viewed as the sum of a differential component and a common-mode component, as

$$V_{in1} = \frac{V_{in1} - V_{in2}}{2} + \frac{V_{in1} + V_{in2}}{2}$$

$$V_{in2} = \frac{V_{in2} - V_{in1}}{2} + \frac{V_{in1} + V_{in2}}{2}$$

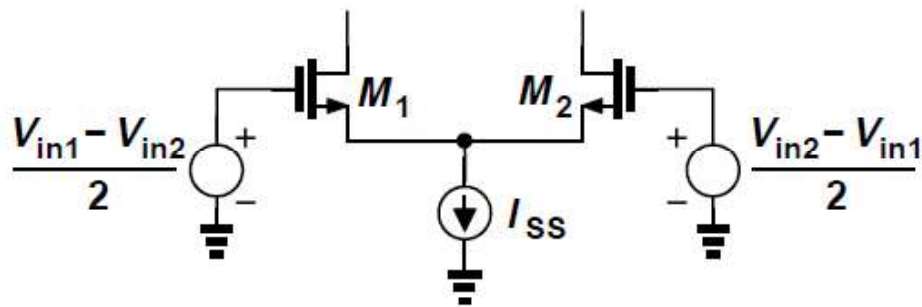
# Half-Circuit Technique



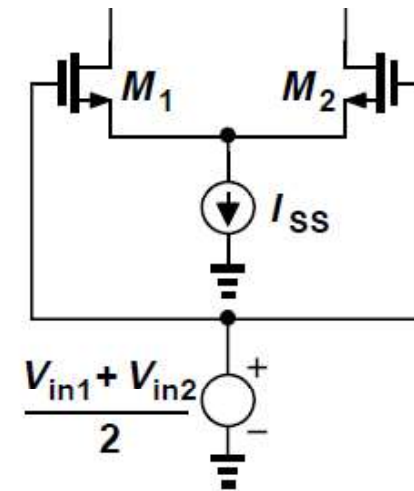
- The circuit can be visualized as shown above
- The circuit senses a combination of a differential input and a common-mode variation
- Effect of each type of input can be computed by superposition, with the half-circuit applied to the differential-mode operation

# Half-Circuit Technique: Example

- Unsymmetrical inputs  $V_{in1}$  and  $V_{in2}$  are superposed as differential [Fig. (a)] and common-mode [Fig. (b)] signals



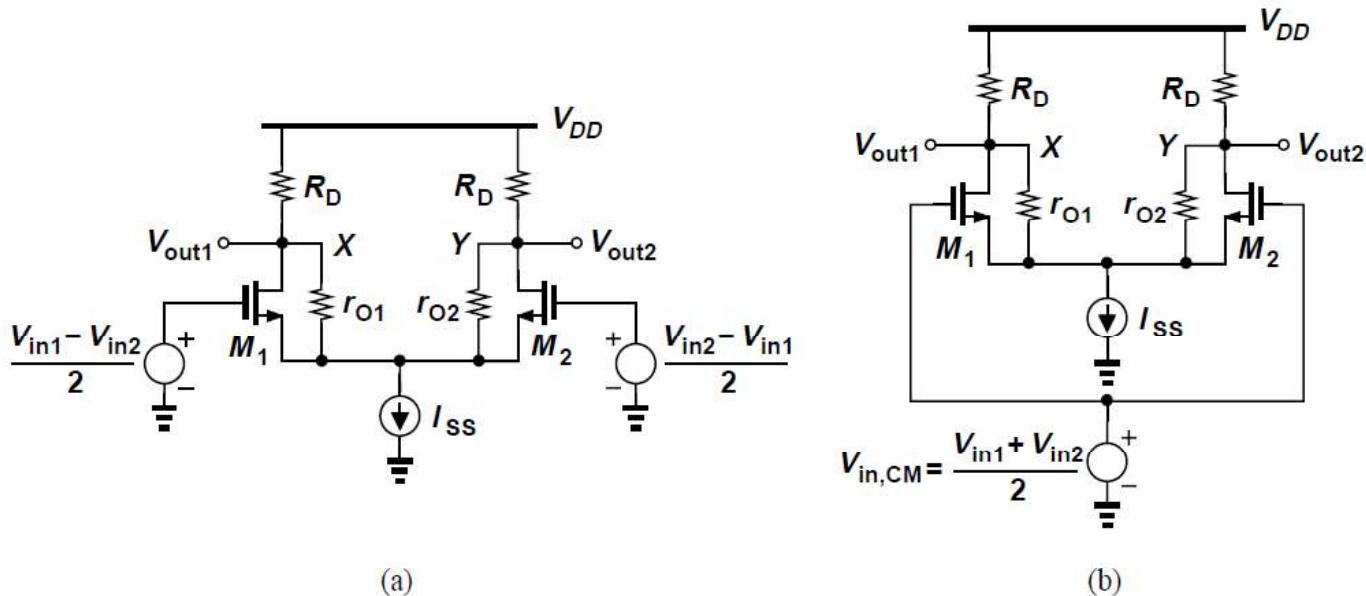
(a)



(b)

# Half-Circuit Technique: Example

- For differential-mode operation, circuit reduces to Fig. (a)



- Thus,

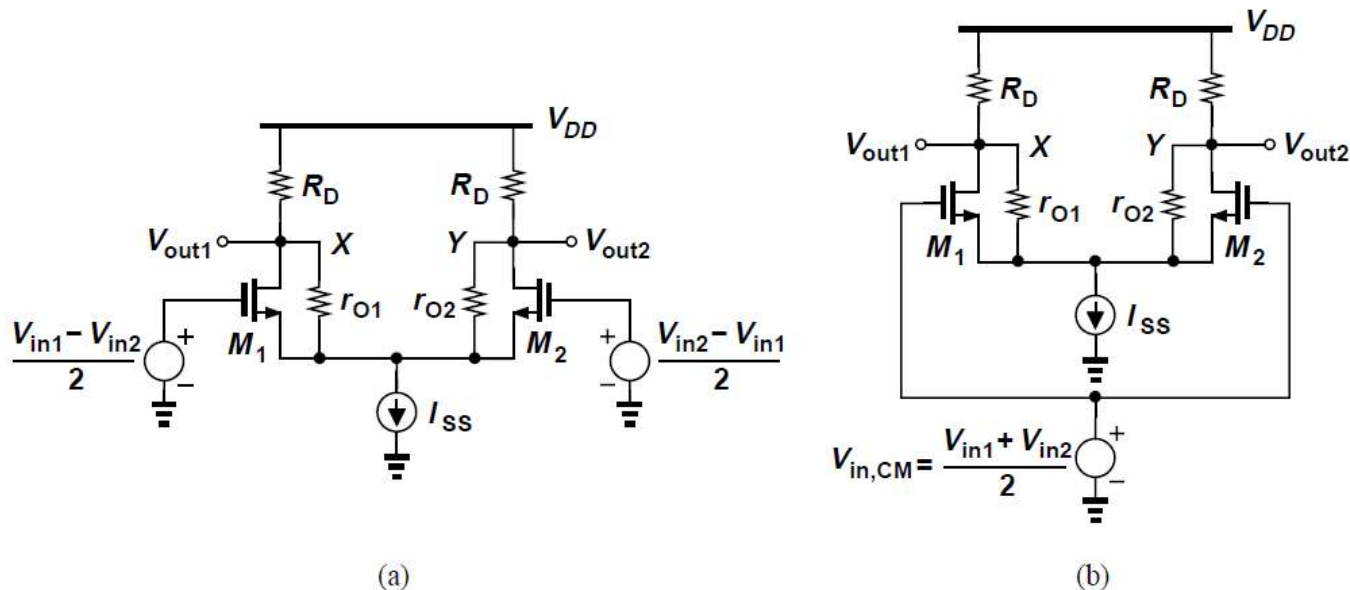
$$V_X = -g_m(R_D \parallel r_{O1}) \frac{V_{in1} - V_{in2}}{2}$$

$$V_Y = -g_m(R_D \parallel r_{O2}) \frac{V_{in2} - V_{in1}}{2}$$

$$V_X - V_Y = -g_m(R_D \parallel r_O)(V_{in1} - V_{in2})$$

# Half-Circuit Technique: Example

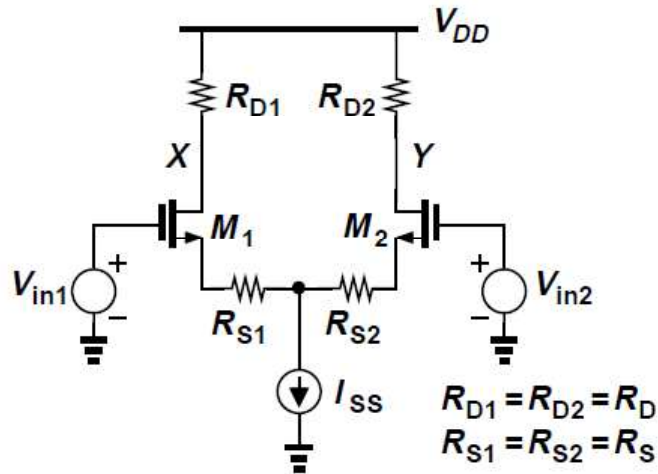
- For common-mode operation, circuit reduces to that in Fig. (b)



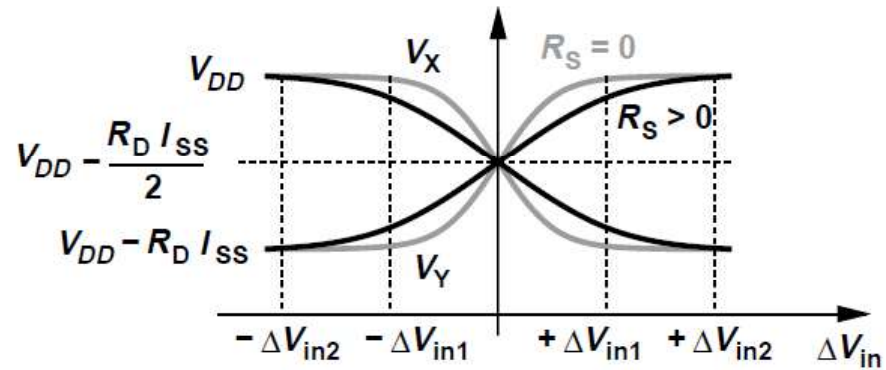
- If circuit is fully symmetric and  $I_{SS}$  is an ideal current source, the currents drawn by  $M_1$  and  $M_2$  from  $R_{D1}$  and  $R_{D2}$  are exactly equal to  $I_{SS}/2$  and independent of  $V_{in,CM}$
- $V_X$  and  $V_Y$  remain equal to  $V_{DD} - R_D(I_{SS}/2)$  and do not vary with  $V_{in,CM}$ , therefore, circuit simply amplifies  $V_{in1} - V_{in2}$  while eliminating the effect  $V_{in,CM}$

# Degenerated Differential Pair

- A differential pair can incorporate resistive degeneration to improve linearity [Fig. (a)]



(a)

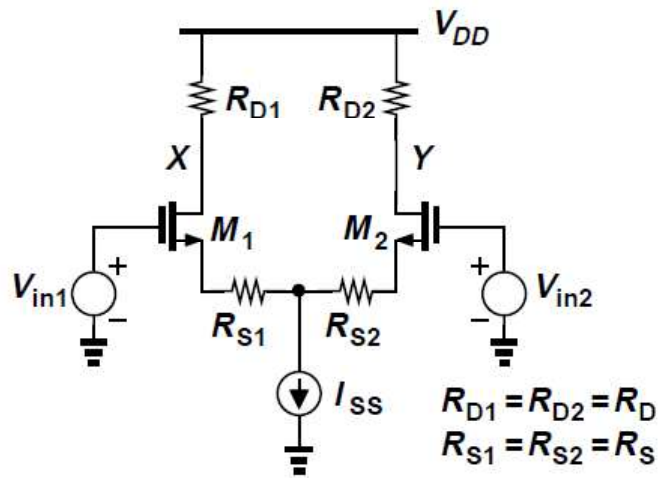


(b)

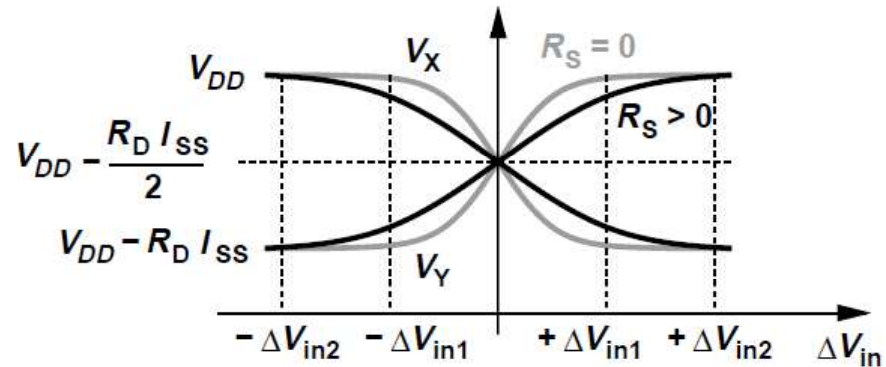
- $R_{S1}$  and  $R_{S2}$  soften the nonlinear behavior of  $M_1$  and  $M_2$  by increasing the differential voltage necessary to turn off one side [Fig. (b)]
- Suppose at  $V_{in1} - V_{in2} = \Delta V_{in2}$ ,  $M_2$  turns off and  $I_{D1} = I_{SS}$ , then  $V_{GS2} = V_{TH}$  and hence

$$V_{in1} - V_{GS1} - R_S I_{SS} = V_{in2} - V_{TH}$$

# Degenerated Differential Pair



(a)



(b)

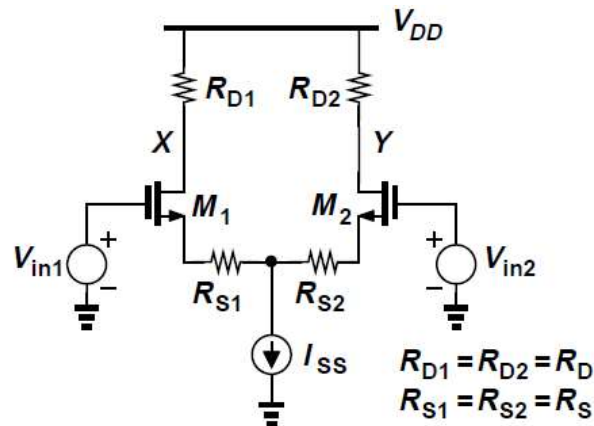
- Thus

$$\begin{aligned}
 V_{in1} - V_{in2} &= V_{GS1} - V_{TH} + R_S I_{SS} \\
 &= \sqrt{\frac{2I_{SS}}{\mu_n C_{ox} \frac{W}{L}}} + R_S I_{SS}
 \end{aligned}$$

- First term on RHS is  $\Delta V_{in1}$ , the input difference needed to turn off  $M_2$  if  $R_S = 0$ , giving  $\Delta V_{in2} - \Delta V_{in1} = R_S I_{SS}$
- Linear input range is widened by approximately  $\pm R_S I_{SS}$

# Degenerated Differential Pair

- The small-signal voltage gain can be found using the half-circuit concept



- The half-circuit is simply a degenerated CS stage exhibiting a gain of

$$|A_v| = \frac{R_D}{\frac{1}{g_m} + R_S}$$

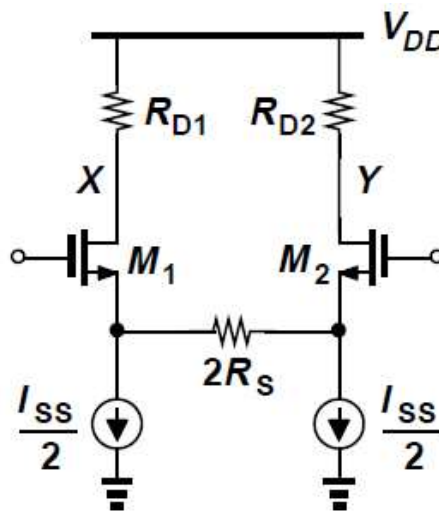
if  $\lambda = \gamma = 0$

- The degenerated circuit trades gain for linearity
- $A_v$  is less sensitive to  $g_m$  variations



# Degenerated Differential Pair

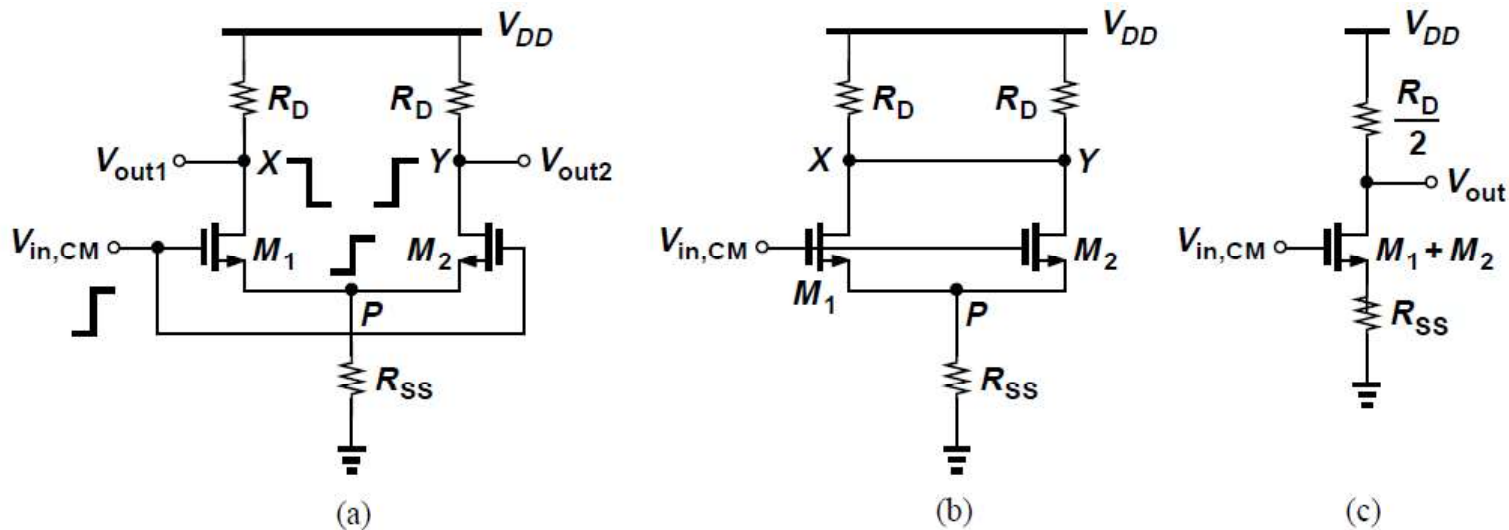
- Degeneration resistors consume voltage headroom
- In equilibrium, each resistor sustains a voltage drop of  $R_S I_{SS}/2$  and maximum allowable differential swing is reduced by  $R_S I_{SS}/2$



- This can be resolved by splitting the tail current source in half and connecting each to the source terminal
- No headroom is sacrificed across the degeneration resistance in equilibrium

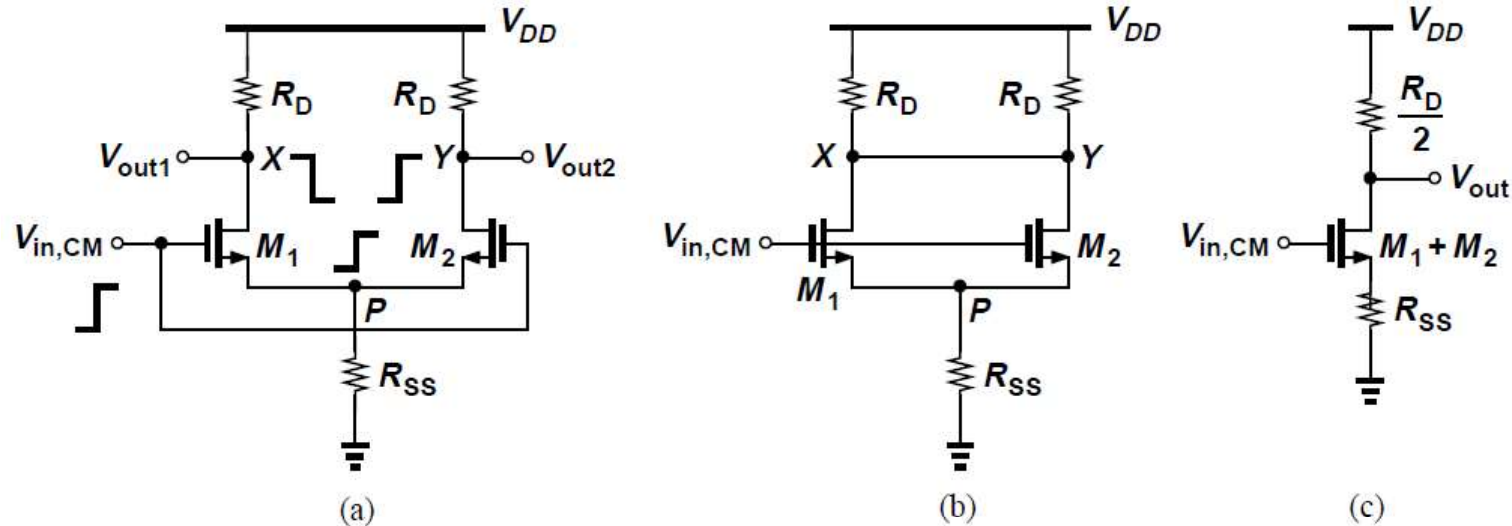
# BASIC DIFFERENTIAL PAIR: Common-Mode Response

- In reality, the differential pair is not fully symmetric and the tail current source exhibits a finite output impedance
- A fraction of the input CM variations appear at the output



- First assume that circuit is symmetric but tail current source has a finite output impedance  $R_{SS}$  [Fig. (a)]
- Increase in  $V_{in,CM}$  causes  $V_P$  to increase and both  $V_X$ ,  $V_Y$  to drop, which remain equal due to symmetry [Fig. (b)]

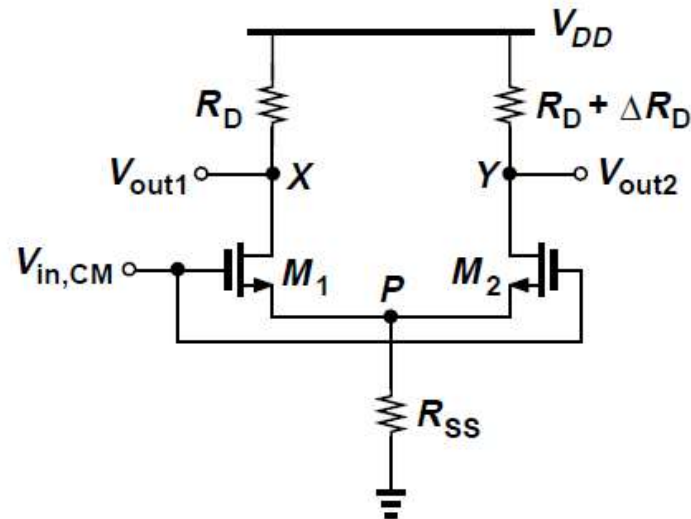
# BASIC DIFFERENTIAL PAIR: Common-Mode Response



- $M_1$  and  $M_2$  are “in parallel” and can be reduced to one composite device with twice the width, bias current and transconductance
- “Common-mode gain” of the circuit is ( $\lambda = \gamma = 0$ )
 
$$A_{v,CM} = \frac{V_{out}}{V_{in,CM}} = -\frac{R_D/2}{1/(2g_m) + R_{SS}}$$
- Input CM variations disturb bias points and affect small-signal gain and output swings

# BASIC DIFFERENTIAL PAIR: Common-Mode Response

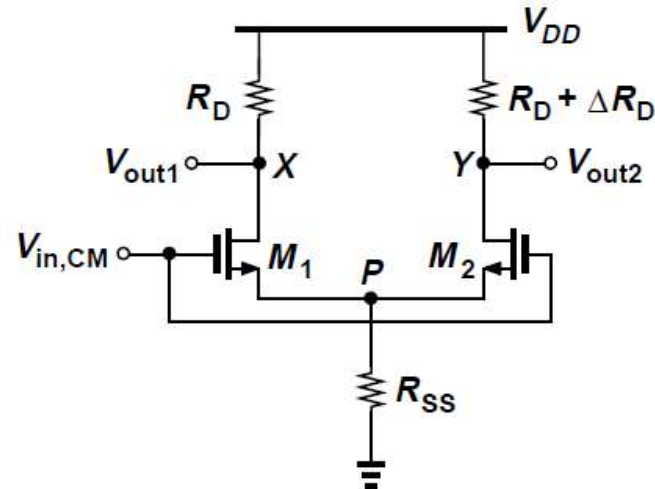
- There is variation in differential output due to change in  $V_{in,CM}$  since the circuit is not fully symmetric, i.e., slight mismatches between the two sides



- $R_{D1} = R_D, R_{D2} = R_D + \Delta R_D$ , where  $\Delta R_D$  denotes a small mismatch and circuit is otherwise symmetric ( $\lambda = \gamma = 0$  for  $M_1$  and  $M_2$ )
- $M_1$  and  $M_2$  operate as one source follower, raising  $V_P$  by

$$\Delta V_P = \frac{R_{SS}}{R_{SS} + \frac{1}{2g_m}} \Delta V_{in,CM}$$

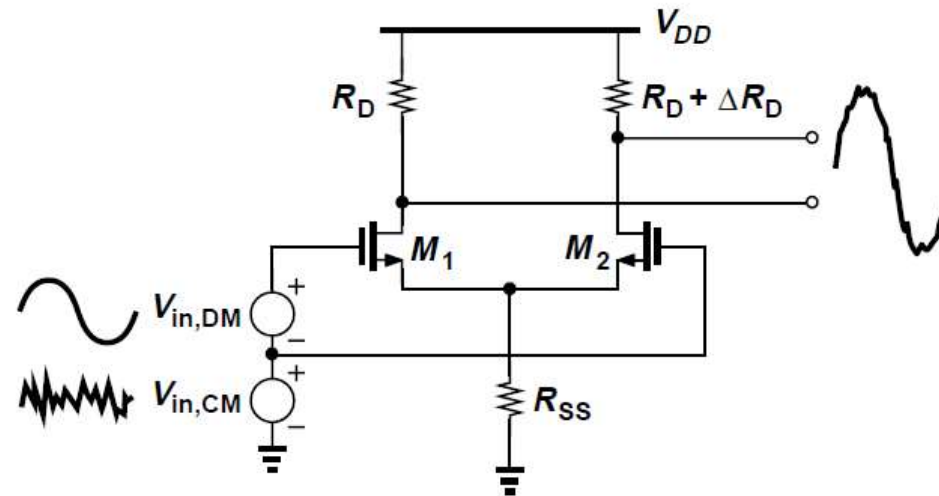
# BASIC DIFFERENTIAL PAIR: Common-Mode Response



- Since  $M_1$  and  $M_2$  are identical,  $I_{D1}$  and  $I_{D2}$  increase by  $[g_m / (1 + 2g_m R_{SS})] \Delta V_{in,CM}$
- $V_X$  and  $V_Y$  change by different amounts
 
$$\Delta V_X = -\Delta V_{in,CM} \frac{g_m}{1 + 2g_m R_{SS}} R_D$$

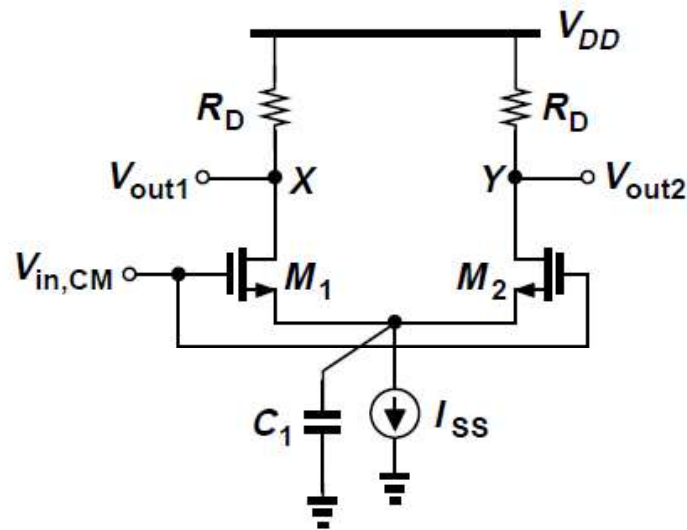
$$\Delta V_Y = -\Delta V_{in,CM} \frac{g_m}{1 + 2g_m R_{SS}} (R_D + \Delta R_D)$$
- Common-mode change at the input introduces a differential component at the output – common-mode to differential conversion

# BASIC DIFFERENTIAL PAIR: Common-Mode Response



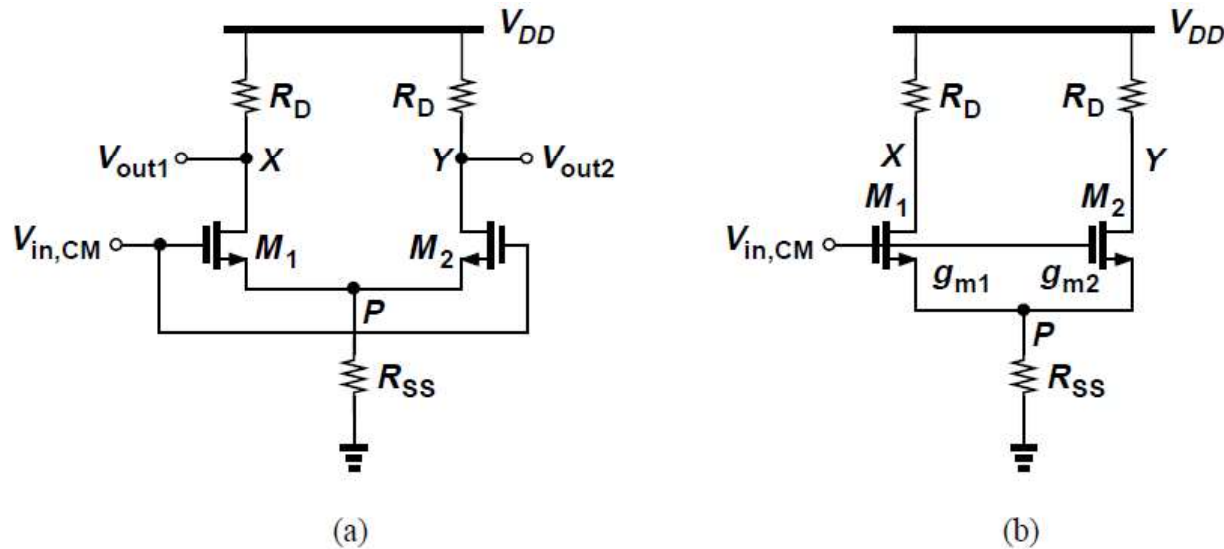
- **Common-mode response depends on output impedance of tail current source and asymmetries in the circuit**
- **Two effects:**
  - **Variation of output CM level (in the absence of mismatches)**
  - **Conversion of input CM variations to output differential components (more severe)**

# Common-mode to differential conversion



- CM to differential conversions become significant at high frequencies since the total capacitance shunting the tail current source introduces larger tail current variations
- This capacitance arises from parasitics of the current source and source-bulk junctions of  $M_1$  and  $M_2$
- Asymmetry in the circuit stems from both the load resistors and the input transistors
  - Latter contributes a greater mismatch

# Common-Mode Response: Transistor Mismatch



- $M_1$  and  $M_2$  exhibit unequal transconductances  $g_{m1}$  and  $g_{m2}$  due to dimension and  $V_{TH}$  mismatches (assume  $\lambda = \gamma = 0$ )
- Calculate small-signal gain from  $V_{in,CM}$  to  $X$  and  $Y$  [Fig. (b)]

$$I_{D1} = g_{m1}(V_{in,CM} - V_P)$$

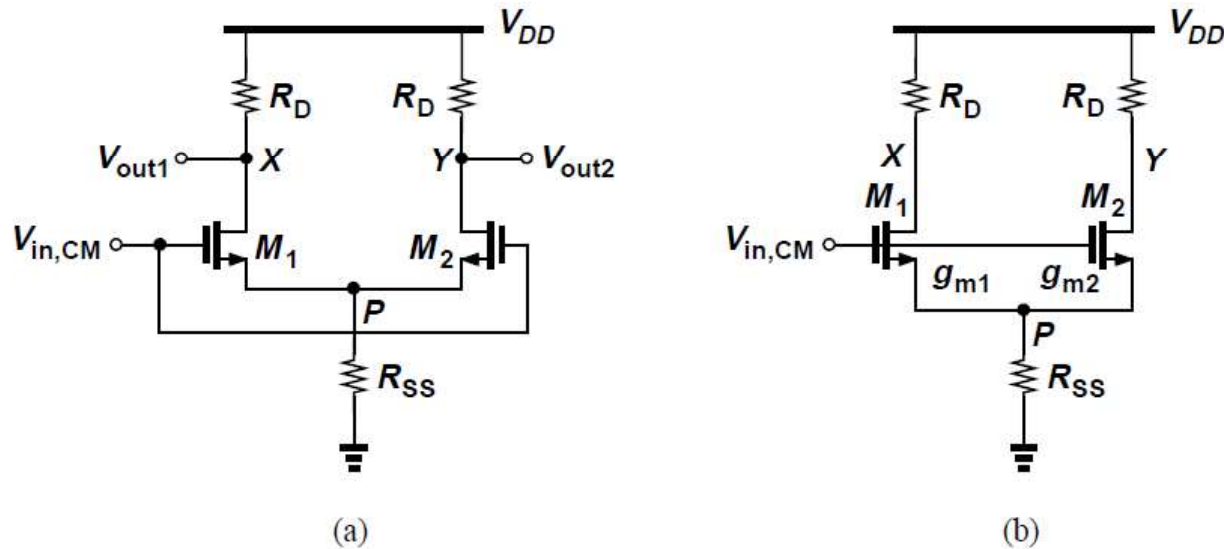
$$I_{D2} = g_{m2}(V_{in,CM} - V_P)$$

- Also,

$$(I_{D1} + I_{D2})R_{SS} = V_P$$



# Common-Mode Response: Transistor Mismatch



- Thus,

$$V_P = \frac{(g_{m1} + g_{m2})R_{SS}}{(g_{m1} + g_{m2})R_{SS} + 1} V_{in,CM}$$

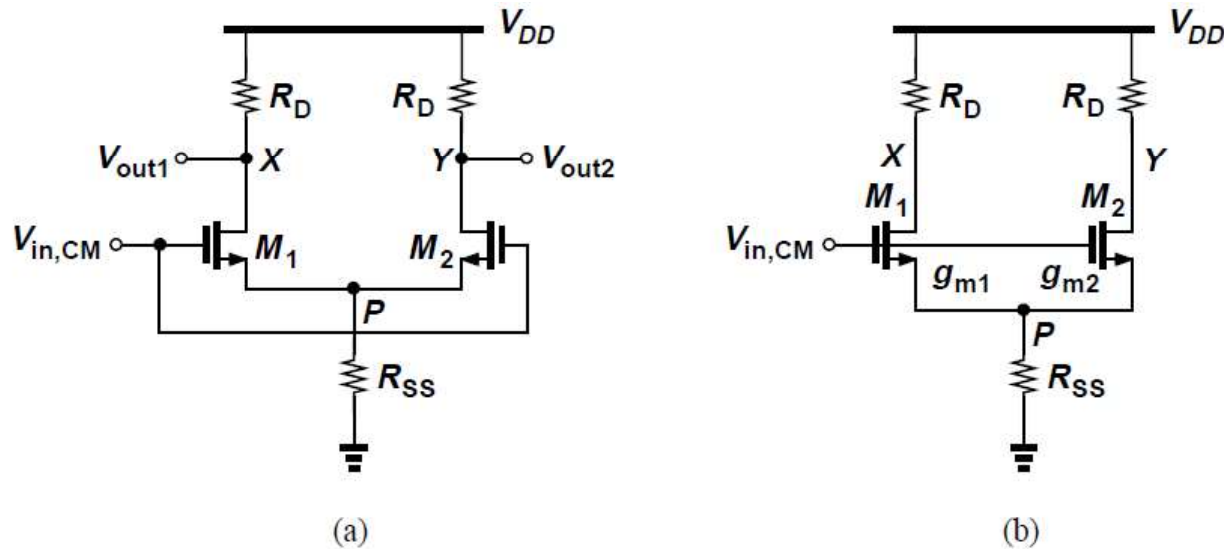
- We now obtain the output voltages as

$$\begin{aligned} V_X &= -g_{m1}(V_{in,CM} - V_P)R_D & V_Y &= -g_{m2}(V_{in,CM} - V_P)R_D \\ &= \frac{-g_{m1}}{(g_{m1} + g_{m2})R_{SS} + 1} R_D V_{in,CM} & &= \frac{-g_{m2}}{(g_{m1} + g_{m2})R_{SS} + 1} R_D V_{in,CM} \end{aligned}$$

- The differential component at the output is

$$V_X - V_Y = -\frac{g_{m1} - g_{m2}}{(g_{m1} + g_{m2})R_{SS} + 1} R_D V_{in,CM}$$

# Common-Mode Response: Transistor Mismatch



- The circuit converts input CM variations to a differential error by a factor of

$$A_{CM-DM} = -\frac{\Delta g_m R_D}{(g_{m1} + g_{m2}) R_{SS} + 1}$$

- $A_{CM-DM}$  denotes common-mode to differential-mode conversion and  $\Delta g_m = g_{m1} - g_{m2}$

# Common-Mode Response

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- Common-mode rejection ratio (CMRR) is defined as the desired gain divided by undesired gain

$$CMRR = \left| \frac{A_{DM}}{A_{CM-DM}} \right|$$

- If only  $g_m$  mismatch is considered, it can be shown that

$$|A_{DM}| = \frac{R_D}{2} \frac{g_{m1} + g_{m2} + 4g_{m1}g_{m2}R_{SS}}{1 + (g_{m1} + g_{m2})R_{SS}}$$

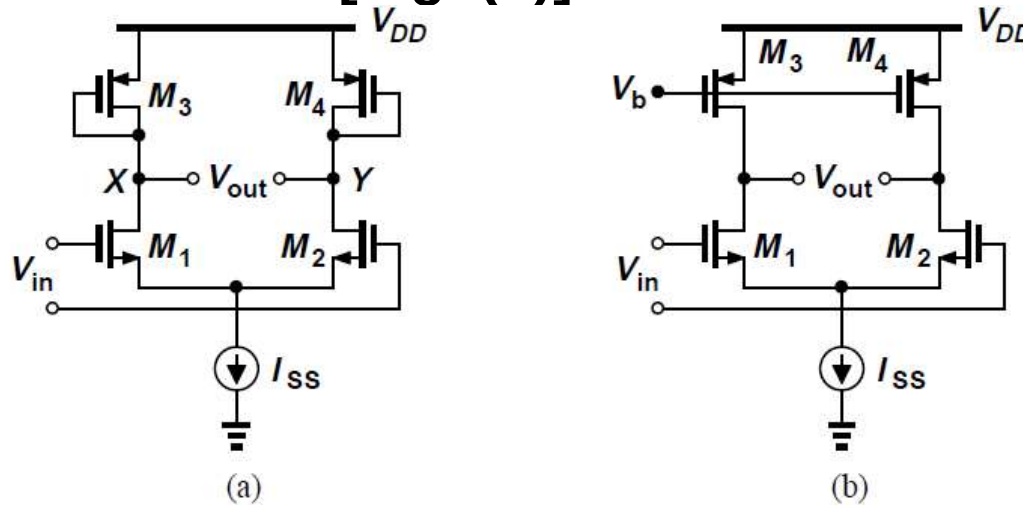
- Hence,

$$\begin{aligned} CMRR &= \frac{g_{m1} + g_{m2} + 4g_{m1}g_{m2}R_{SS}}{2\Delta g_m} \\ &\approx \frac{g_m}{\Delta g_m} (1 + 2g_m R_{SS}), \end{aligned}$$

- $g_m$  denotes the mean value, i.e.,  $g_m = (g_{m1} + g_{m2})/2$
- $2g_m R_{SS} \gg 1$  and hence  $CMRR \approx 2g_m^2 R_{SS} / \Delta g_m$ .

# Differential Pair with MOS Loads

- Differential pairs can employ diode-connected [Fig. (a)] or current-source loads [Fig. (b)]



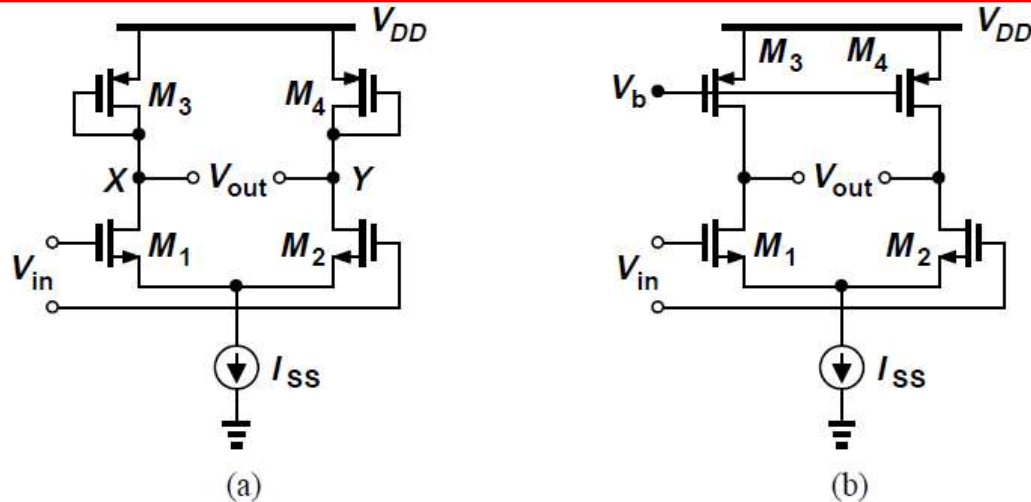
- For Fig. (a), small-signal differential gain is

$$A_v = -g_{mN} \left( g_{mP}^{-1} \parallel r_{ON} \parallel r_{OP} \right)$$

$$\approx -\frac{g_{mN}}{g_{mP}}$$

- $N$  and  $P$  subscripts denote NMOS and PMOS respectively

# Differential Pair with MOS Loads



- Expressing  $g_{mN}$  and  $g_{mP}$  in terms of device dimensions,

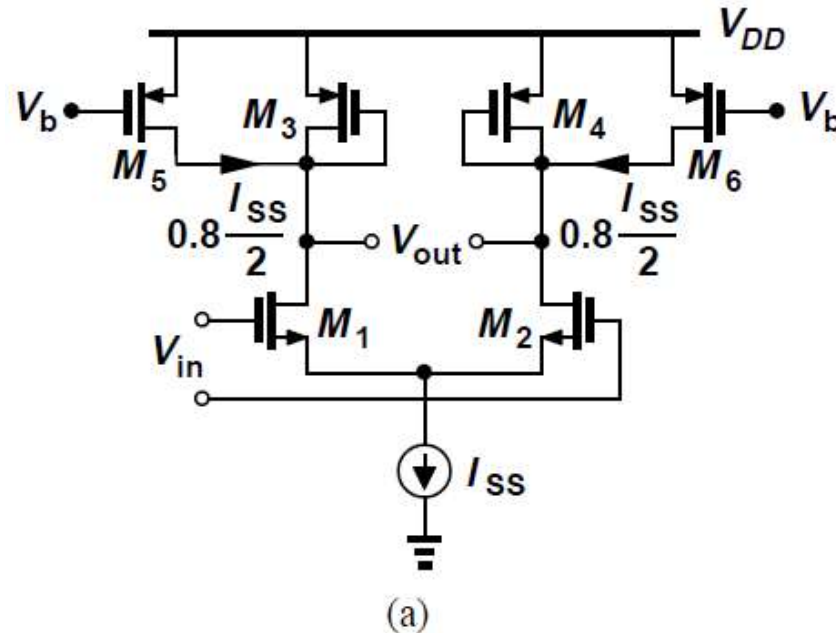
$$A_v \approx -\sqrt{\frac{\mu_n(W/L)_N}{\mu_p(W/L)_P}}$$

- For current-source loads [Fig. (b)], the gain is

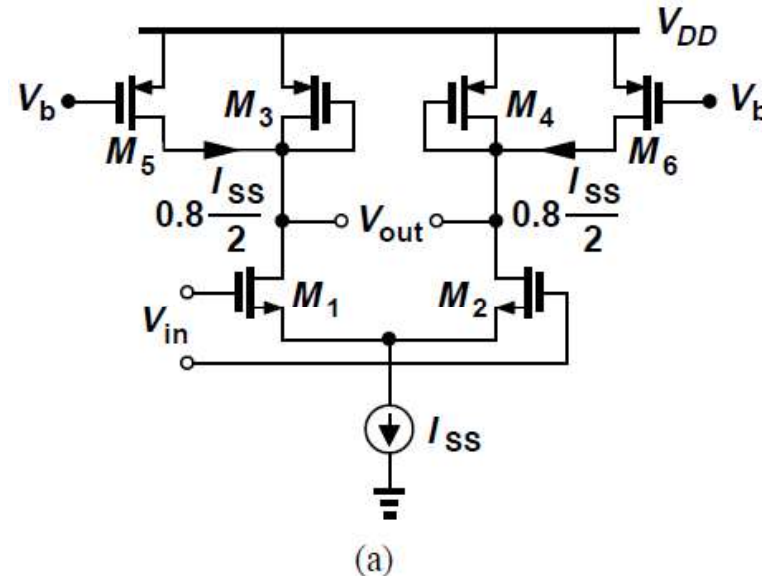
$$A_v = -g_{mN}(r_{ON} || r_{OP})$$

# Differential Pair with MOS Loads

- Diode-connected loads consume voltage headroom and create trade-off between output voltage swing, input CM range and gain
- For higher gain,  $(W/L)_p$  must decrease, thereby increasing  $|V_{GS} - V_{THP}|$  and lowering output CM level
- Solved by adding PMOS current sources  $M_5$  and  $M_6$  to supply part of input pair bias current [Fig. (a)]



# Differential Pair with MOS Loads

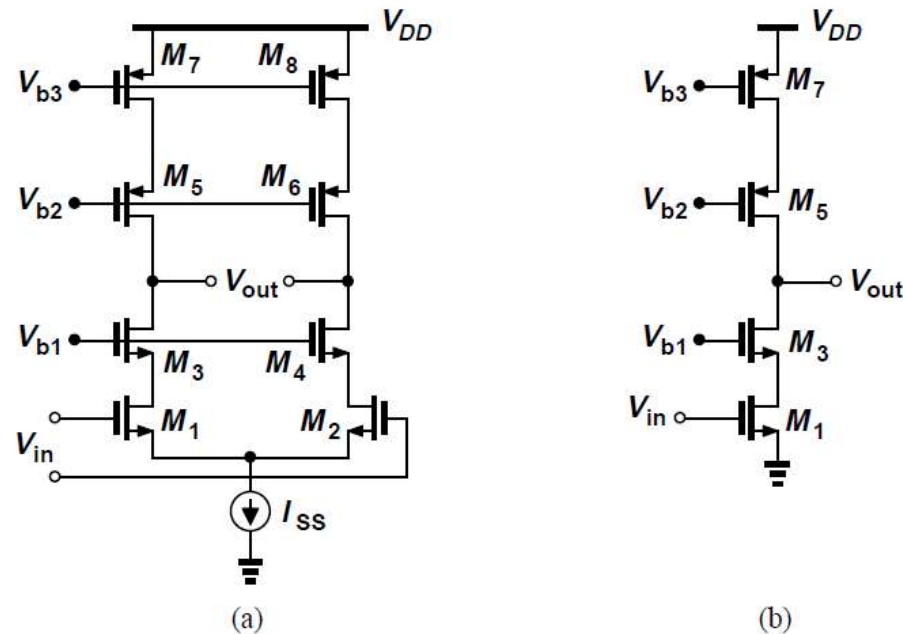


- In Fig. (a),  $g_m$  of load devices  $M_3$  and  $M_4$  is lowered by reducing their current instead of  $(W/L)_p$
- For  $I_{D5} = I_{D6} = 0.8I_{D1} = 0.8I_{D2}$ ,  $I_{D3}$  and  $I_{D4}$  are reduced by a factor of 5
- For a given overdrive,  $g_{mP}$  is lowered by the same factor
- Differential gain is five times that of the case without auxiliary PMOS current sources (if  $\lambda = 0$ )





# Cascode Differential Pair

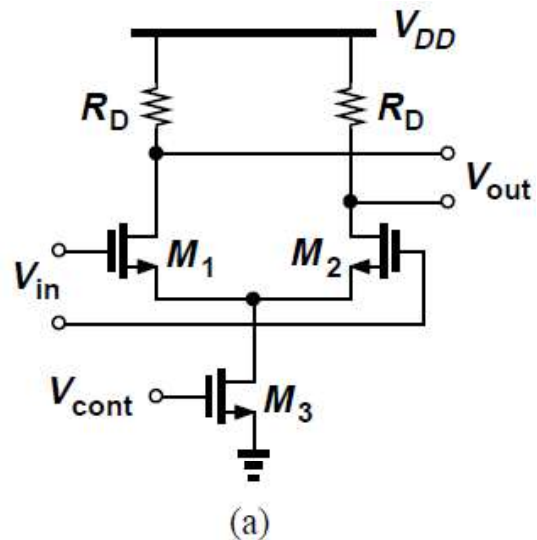


- Small-signal voltage gain can be increased by increasing output impedance of both NMOS and PMOS devices via cascoding [Fig. (a)], but at the cost of less headroom
- The gain is calculated using the half-circuit technique [Fig. (b)]

$$|A_v| \approx g_{m1} [(g_{m3} r_{O3} r_{O1}) || (g_{m5} r_{O5} r_{O7})]$$

# Gilbert Cell

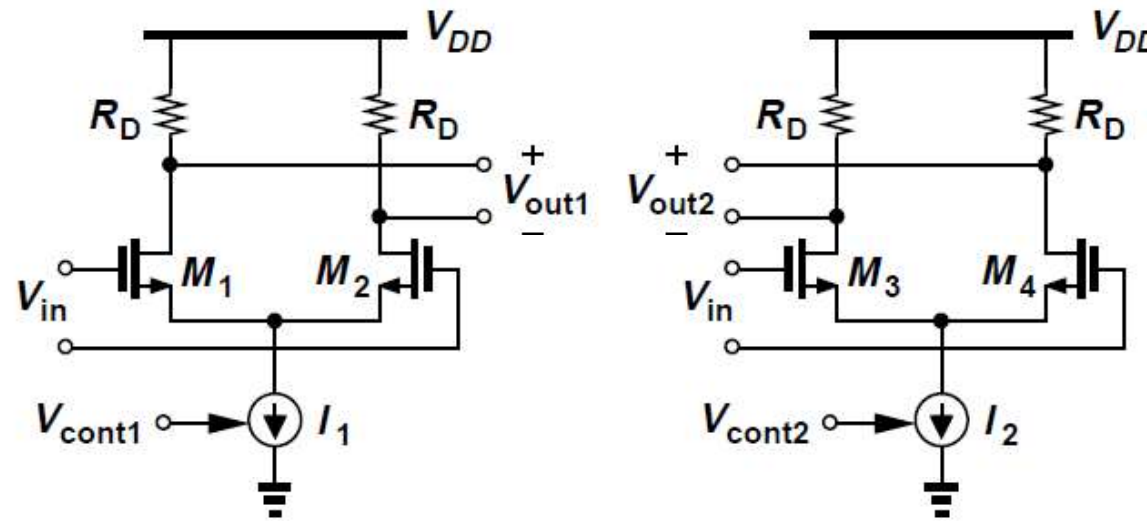
- Differential pair whose gain is controlled by a control voltage [Fig. (a)]



- In Fig.(a), the control voltage  $V_{cont}$  controls the tail current and hence the gain
- Here,  $A_v = V_{out} / V_{in}$  varies from zero (if  $I_{D3} = 0$ ) to a maximum value given by voltage headroom limitations and device dimensions
- Simple example of Variable Gain Amplifier (VGA)

# Gilbert Cell

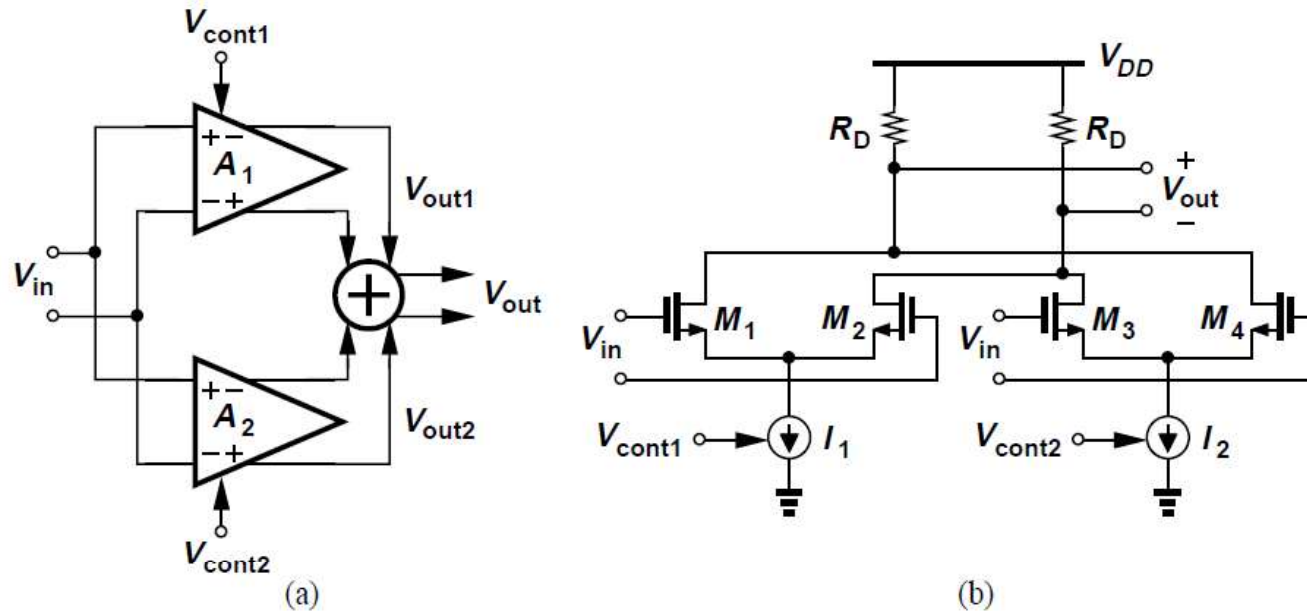
- An amplifier is sought whose gain can be continuously varied from a negative to a positive value



(b)

- Fig. (b) shows two differential pairs that amplify the input by opposite gains
- Here,  $V_{out1}/V_{in} = -g_m R_D$  and  $V_{out2}/V_{in} = +g_m R_D$
- If  $I_1$  and  $I_2$  vary in opposite directions, so do  $|V_{out1}/V_{in}|$  and  $|V_{out2}/V_{in}|$

# Gilbert Cell



- $V_{out1}$  and  $V_{out2}$  are combined into a single output as shown in Fig. (a)
- The two voltages are summed, producing  $V_{out} = V_{out1} + V_{out2} = A_1 V_{in} + A_2 V_{in}$ , where  $A_1$  and  $A_2$  are controlled by  $V_{cont1}$  and  $V_{cont2}$  respectively
- Actual implementation shown in Fig. (b) where drain terminals are shorted to sum the currents and generate the output voltage



