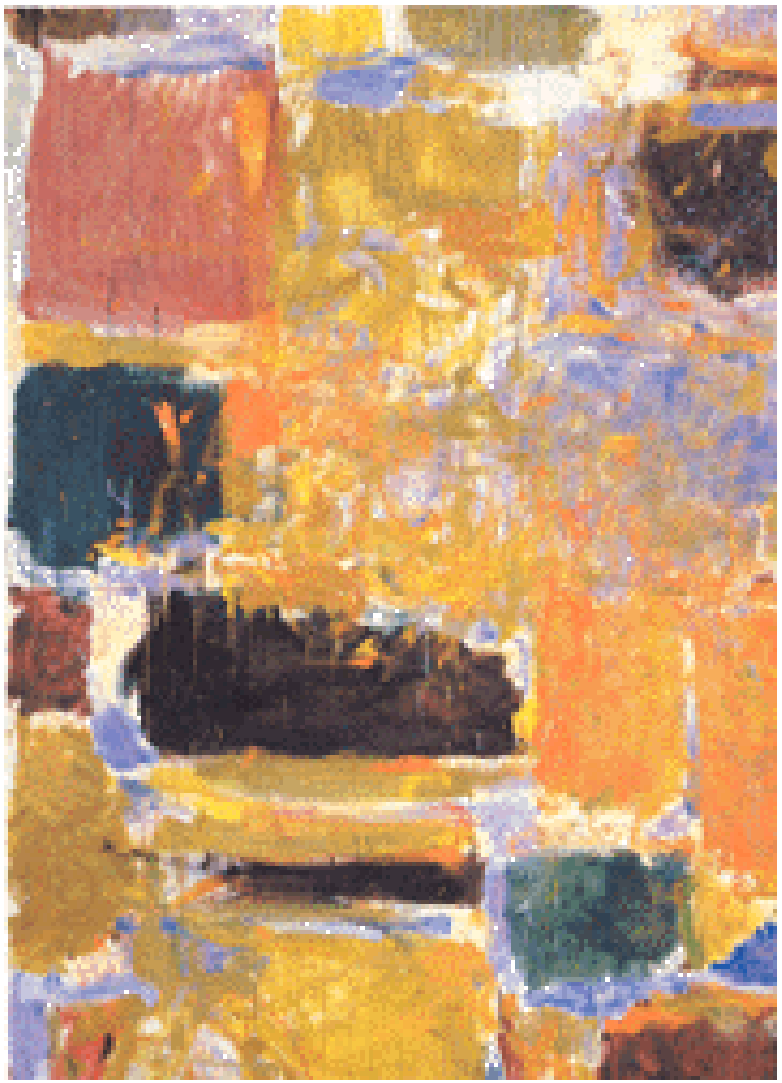
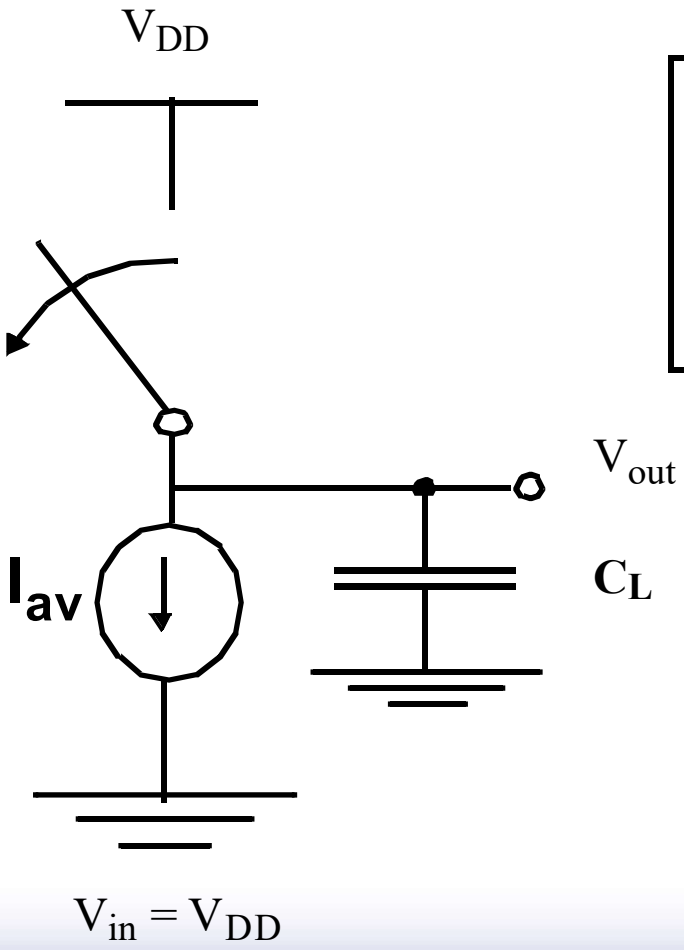


Propagation Delay

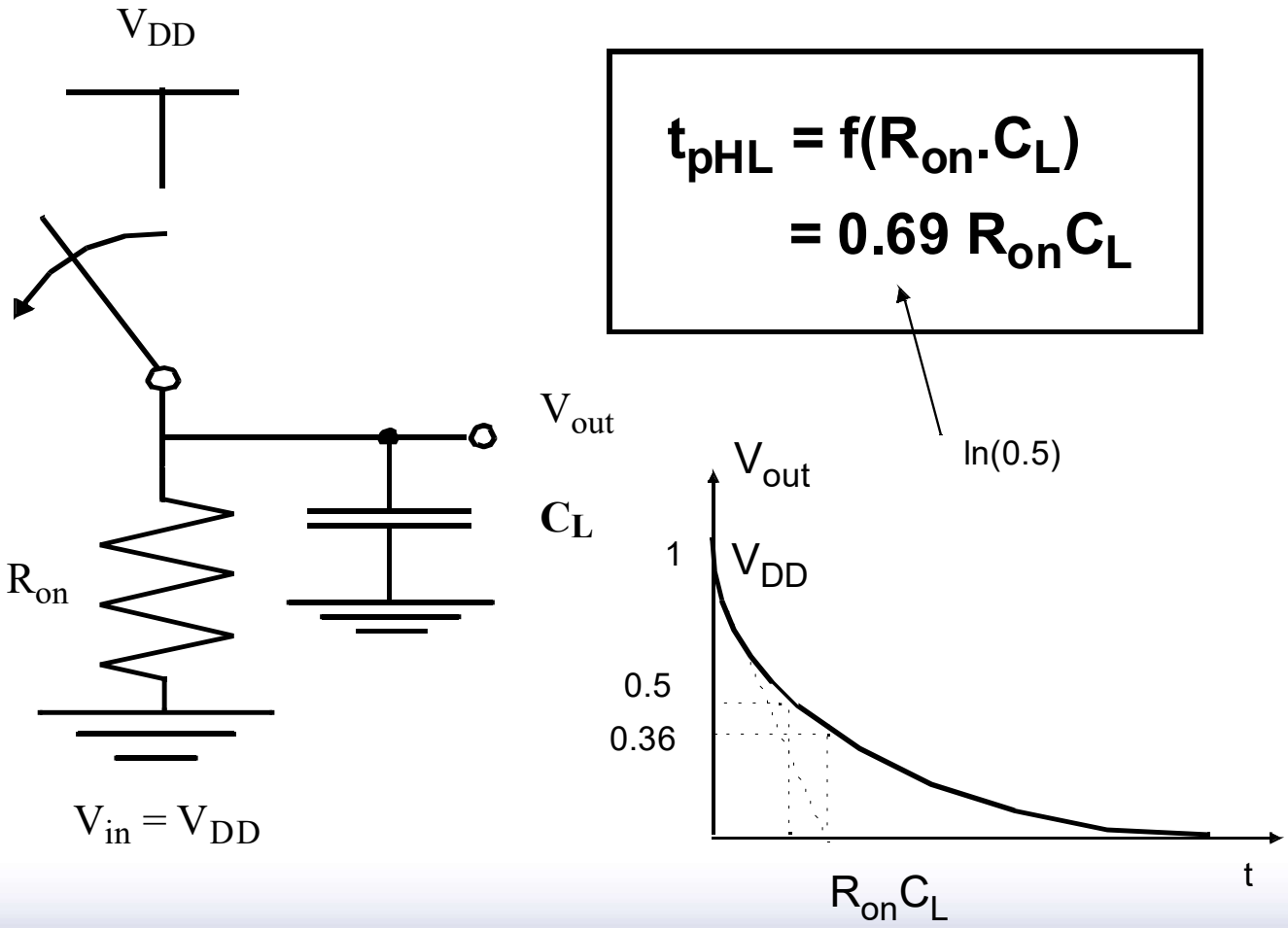
CMOS Inverter Propagation Delay Approach 1



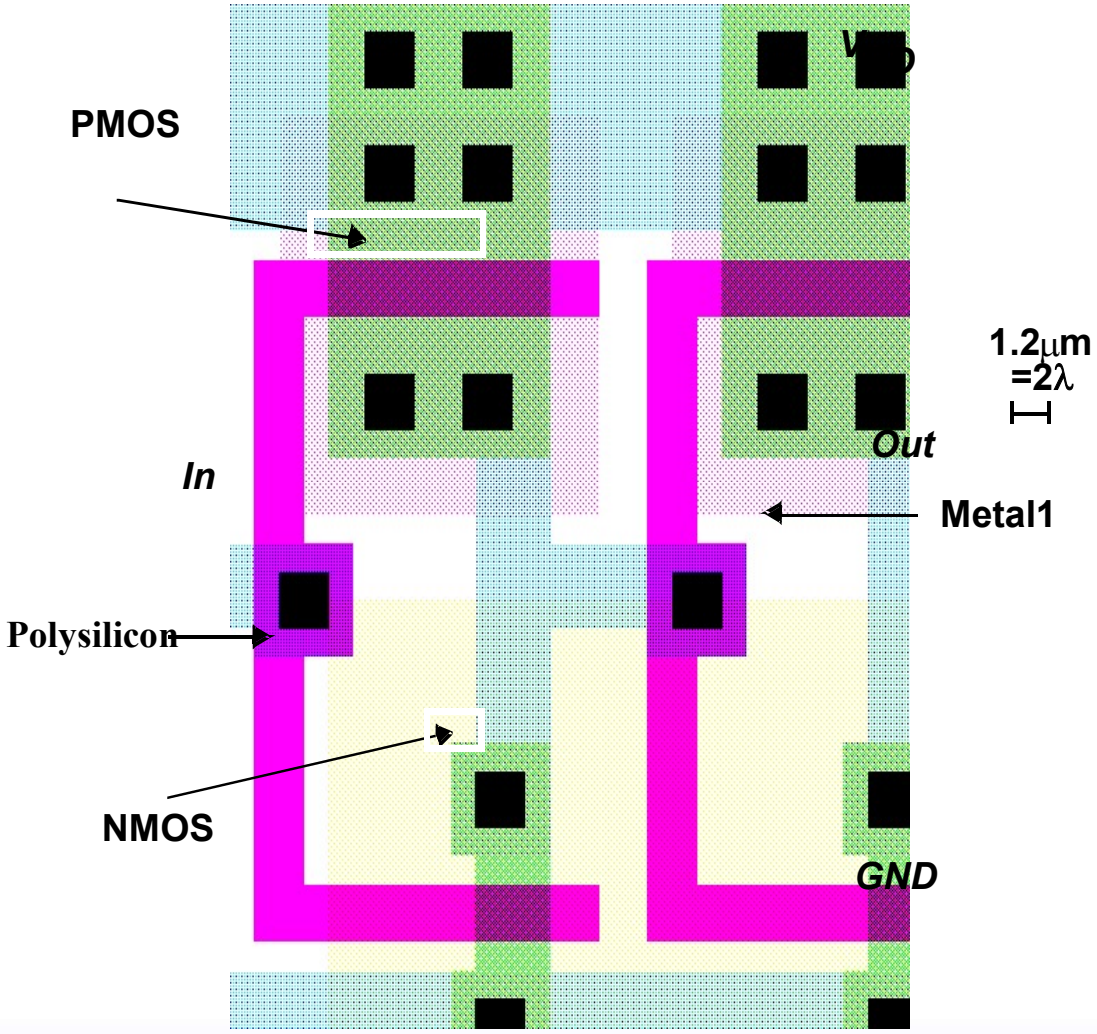
$$t_{pHL} = \frac{C_L V_{swing}/2}{I_{av}}$$

$$\sim \frac{C_L}{k_n V_{DD}}$$

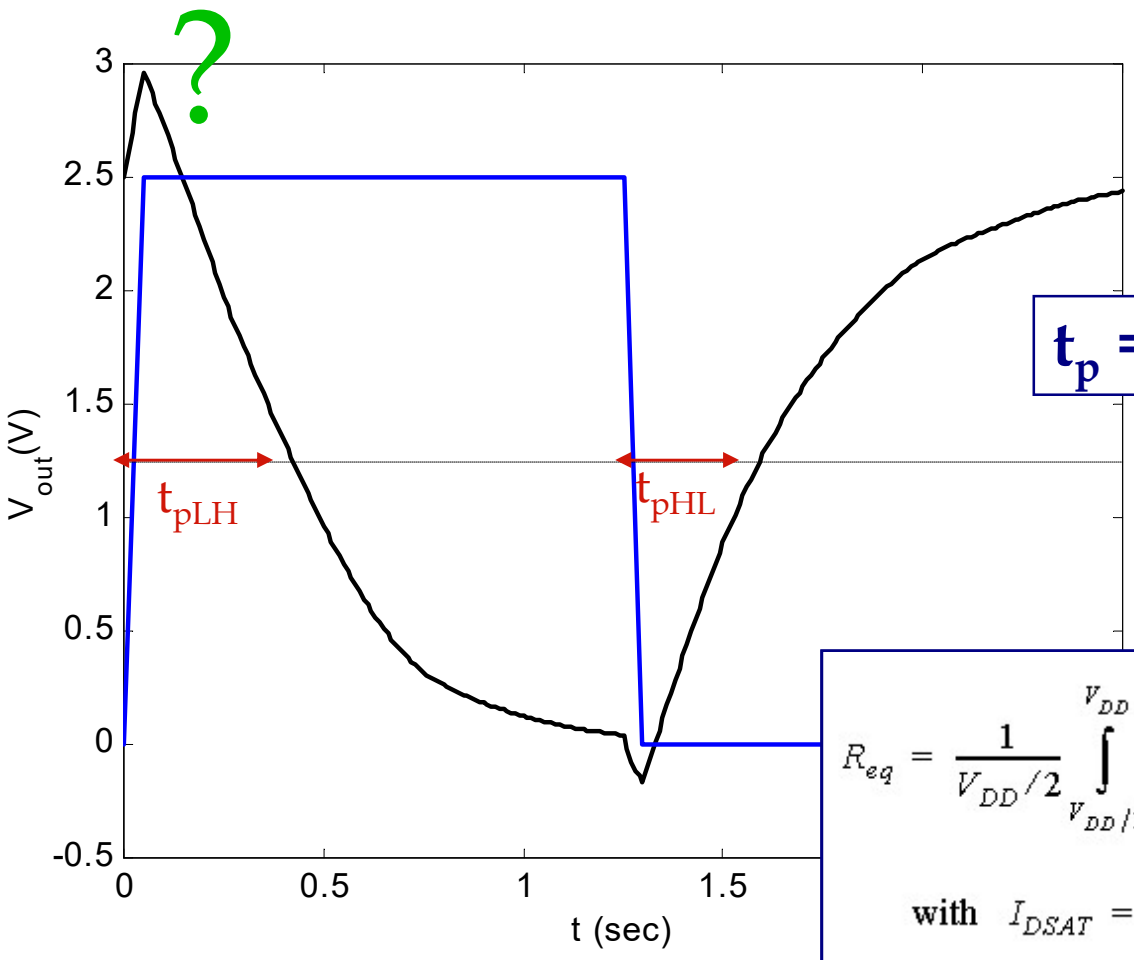
CMOS Inverter Propagation Delay Approach 2



CMOS Inverters



Transient Response



$$t_p = 0.69\, C_L\, (R_{eqn}+R_{eqp})/2$$

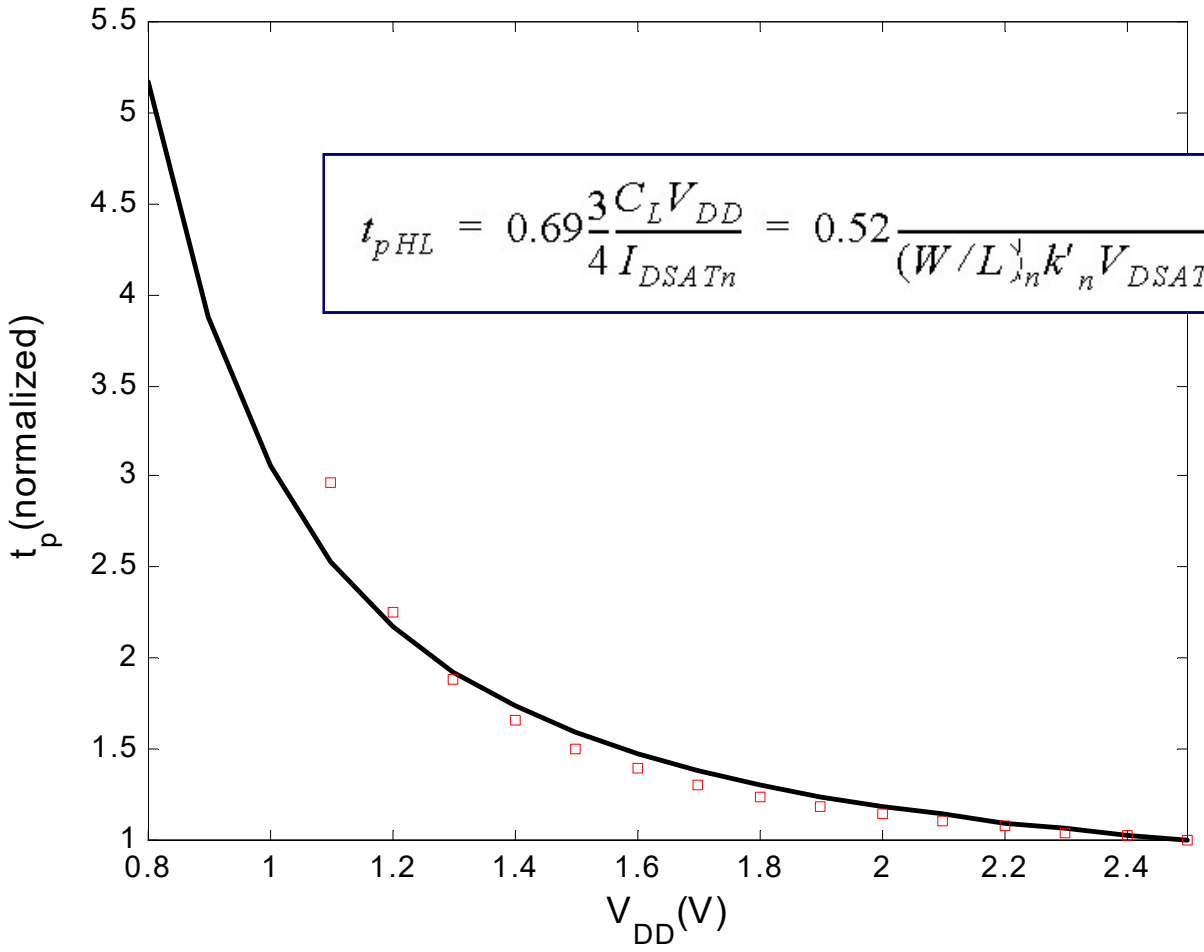
$$R_{eq} = \frac{1}{V_{DD}/2}\int_{V_{DD}/2}^{V_{DD}} \frac{V}{I_{DSAT}(1+\lambda V)}dV \approx \frac{3}{4}\frac{V_{DD}}{I_{DSAT}}\left(1-\frac{7}{9}\lambda V_{DD}\right)$$

with $$I_{DSAT} = k'\frac{W}{L}\left((V_{DD}-V_T)V_{DSAT}-\frac{V_{DSAT}^2}{2}\right)$$

Design for Performance

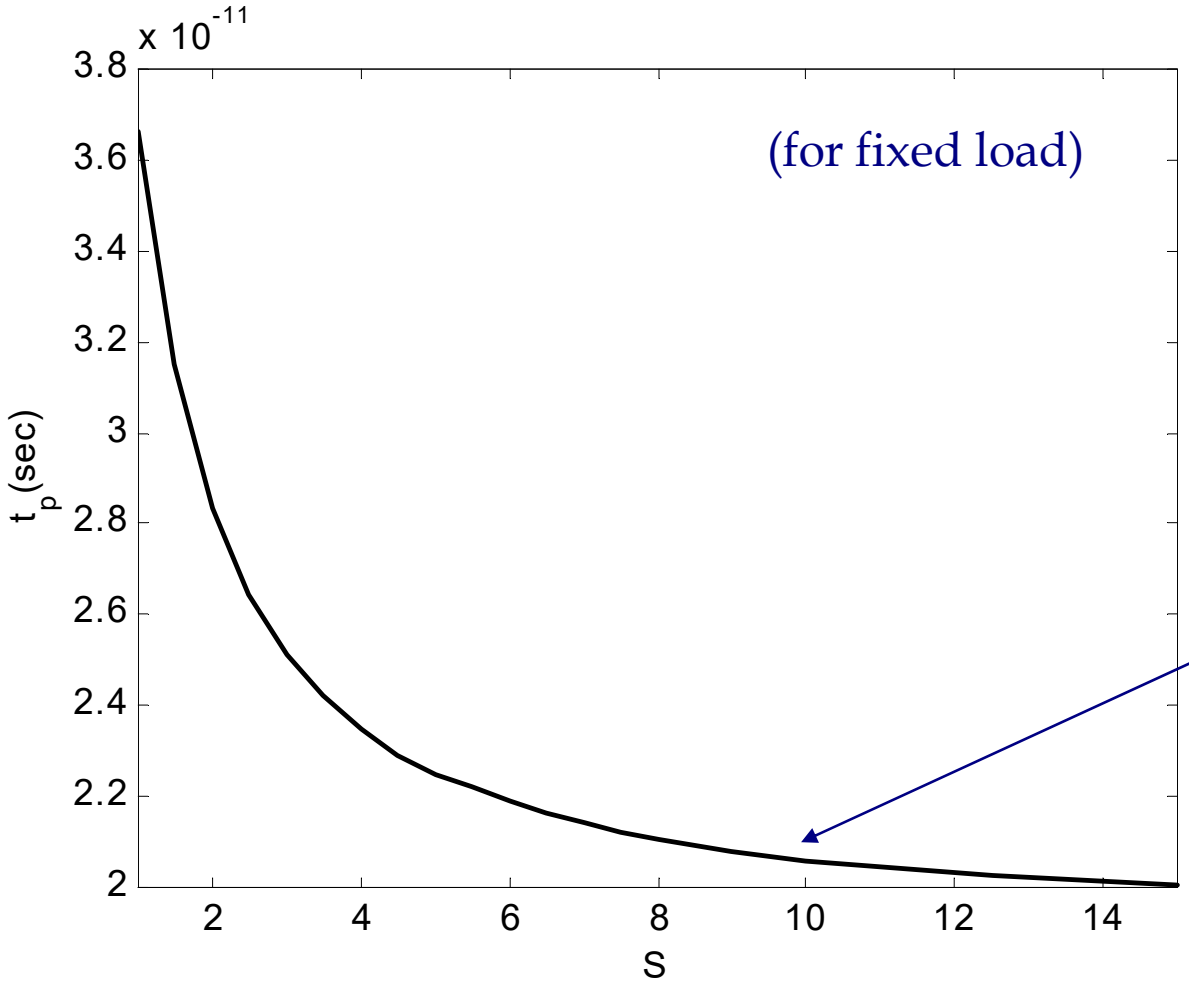
- Keep capacitances small
- Increase transistor sizes
  - watch out for self-loading!
- Increase V_{DD} (????)

Delay as a function of V_{DD}



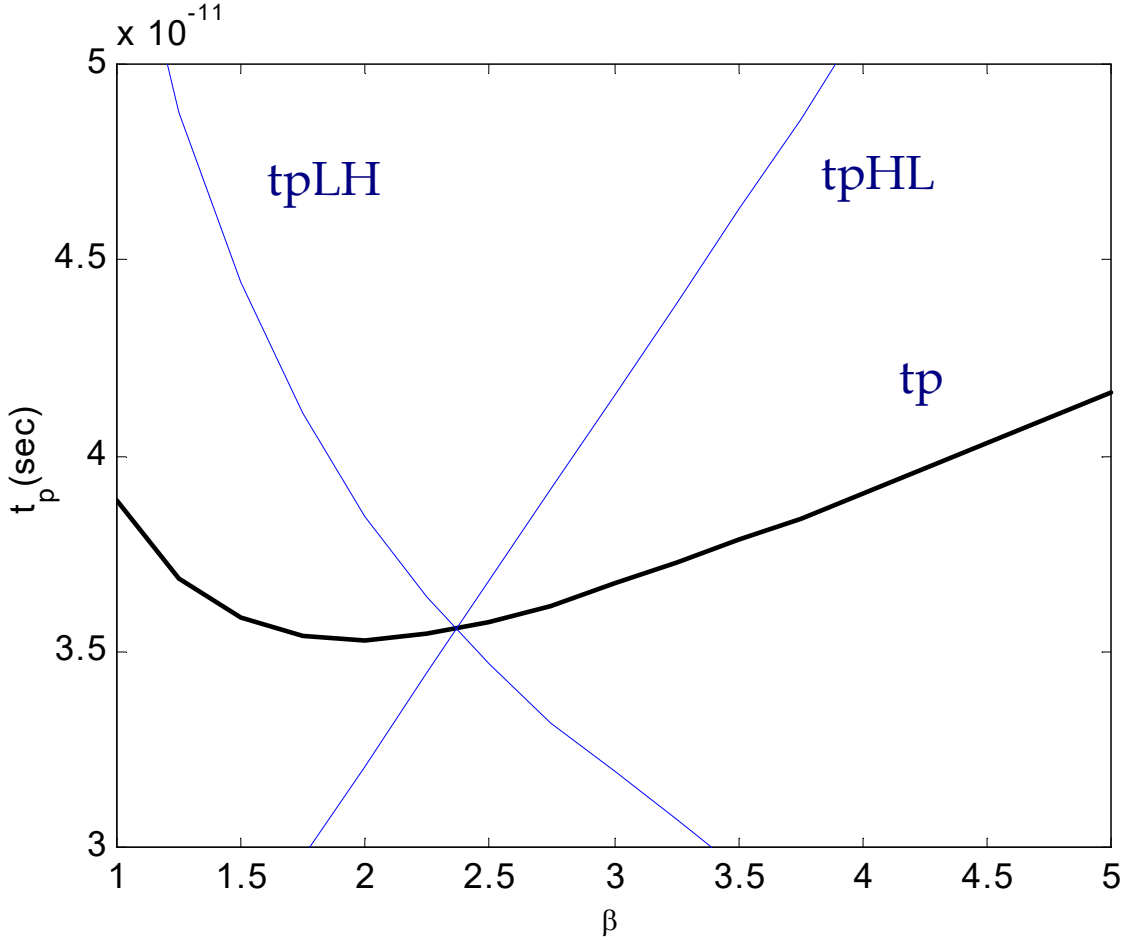
$$t_{pHL} = 0.69\frac{3}{4}\frac{C_L V_{DD}}{I_{DSATn}} = 0.52\frac{C_L V_{DD}}{(W/L)_n k'_n V_{DSATn}(V_{DD} - V_{Tn} - V_{DSATn}/2)}$$

Device Sizing



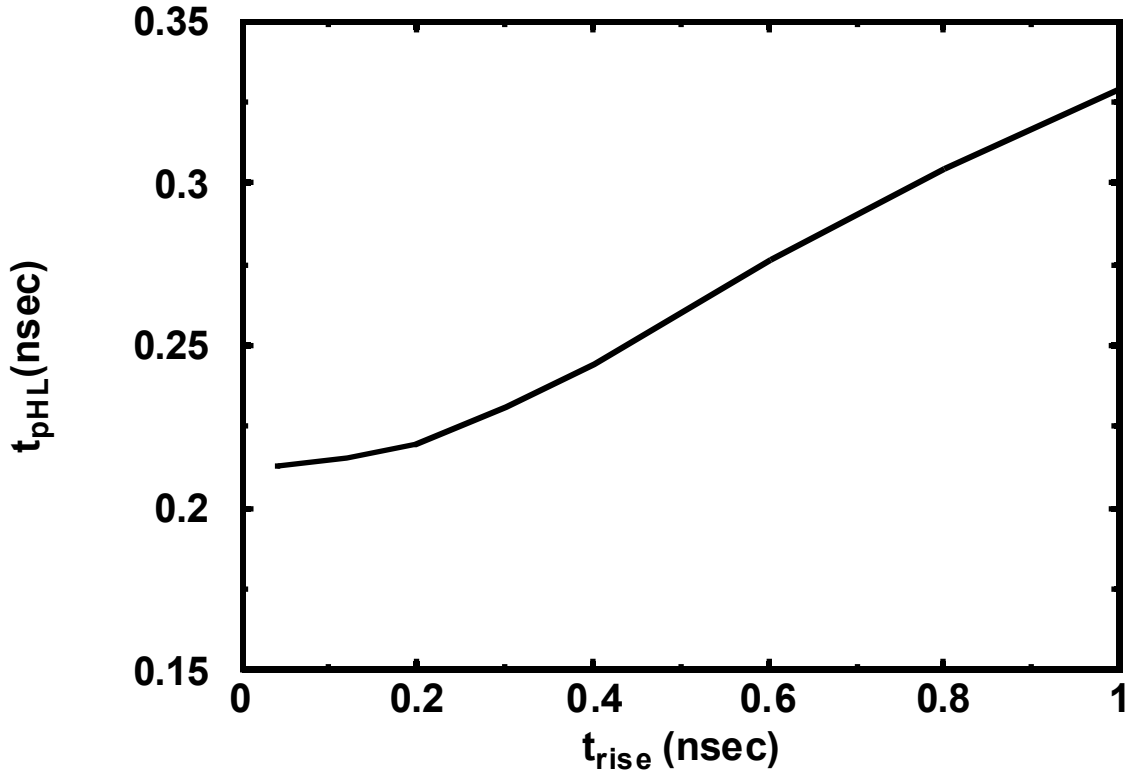
Self-loading effect:
Intrinsic capacitances dominate

NMOS/PMOS ratio



$\beta = W_p/W_n$

Impact of Rise Time on Delay



$$t_{pHL} = \sqrt{t_{pHL(step)}^2 + (t_r/2)^2}$$