
LECTURE 23 – DESIGN OF TWO-STAGE OP AMPS

LECTURE OUTLINE

Outline

- Steps in Designing an Op Amp
- Design Procedure for a Two-Stage Op Amp
- Design Example of a Two-Stage Op Amp
- Right Half Plane Zero
- PSRR of the Two-Stage Op Amp
- Summary

CMOS Analog Circuit Design, 3rd Edition Reference

Pages 286-309

STEPS IN DESIGNING A CMOS OP AMP

Design Inputs

Boundary conditions:

1. Process specification (V_T , K' , C_{ox} , etc.)
2. Supply voltage and range
3. Supply current and range
4. Operating temperature and range

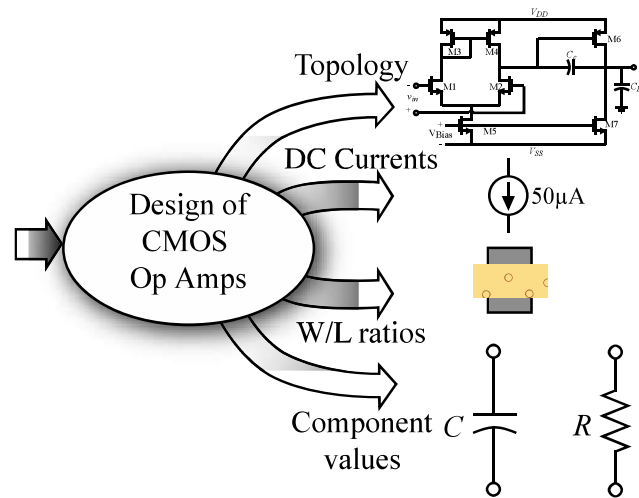
Requirements:

1. Gain
2. Gain bandwidth
3. Settling time
4. Slew rate
5. Common-mode input range, $ICMR$
6. Common-mode rejection ratio, $CMRR$
7. Power-supply rejection ratio, $PSRR$
8. Output-voltage swing
9. Output resistance
10. Offset
11. Noise
12. Layout area

Outputs of Op Amp Electrical Design

The basic outputs are:

- 1.) The topology
- 2.) The dc currents
- 3.) The W and L values of transistors
- 4.) The values of components



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Some Practical Thoughts on Op Amp Design

- 1.) Decide upon a suitable topology.
 - Experience is a great help
 - The topology should be the one capable of meeting most of the specifications
 - Try to avoid “inventing” a new topology but start with an existing topology
- 2.) Determine the type of compensation needed to meet the specifications.
 - Consider the load and stability requirements
 - Use some form of Miller compensation or a self-compensated approach
- 3.) Design dc currents and device sizes for proper dc, ac, and transient performance.
 - This begins with hand calculations based upon approximate design equations.
 - Compensation components are also sized in this step of the procedure.
 - After each device is sized by hand, a circuit simulator is used to fine tune the design

Two basic steps of design:

- 1.) “First-cut” - this step is to use hand calculations to propose a design that has potential of satisfying the specifications. Design robustness is developed in this step.
- 2.) Optimization - this step uses the computer to refine and optimize the design.

A DESIGN PROCEDURE FOR THE TWO-STAGE CMOS OP AMP

Unbuffered, Two-Stage CMOS Op Amp

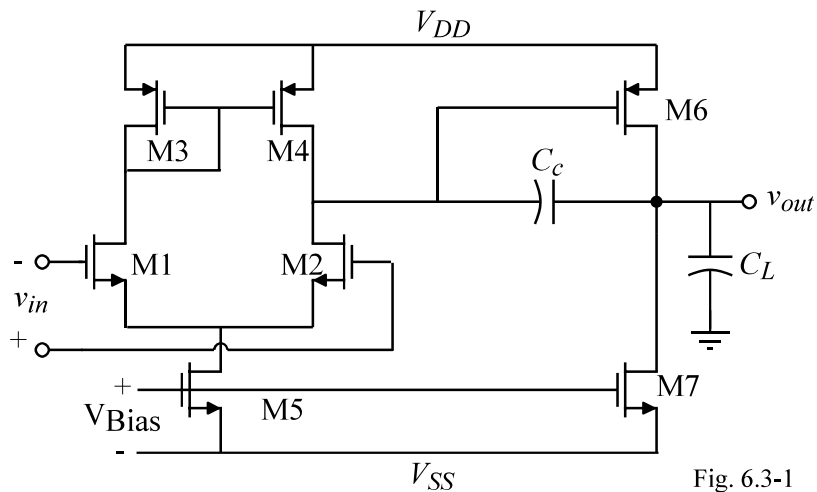


Fig. 6.3-1

Notation:

$$S_i = \frac{W_i}{L_i} = W/L \text{ of the } i\text{th transistor}$$

Summary of the Design Relationships for the Two-Stage Op Amp

$$\text{Slew rate } SR = \frac{I_5}{C_c} \text{ (Assuming } I_7 \gg I_5 \text{ and } C_L > C_c)$$

$$\text{First-stage gain } A_{v1} = \frac{g_{m1}}{g_{ds2} + g_{ds4}} = \frac{2g_{m1}}{I_5(l_2 + l_4)}$$

$$\text{Second-stage gain } A_{v2} = \frac{g_{m6}}{g_{ds6} + g_{ds7}} = \frac{g_{m6}}{I_6(l_6 + l_7)}$$

$$\text{Gain-bandwidth } GB = \frac{g_{m1}}{C_c}$$

$$\text{Output pole } p_2 = \frac{-g_{m6}}{C_L}$$

$$\text{RHP zero } z_1 = \frac{g_{m6}}{C_c}$$

60° phase margin requires that $g_{m6} = 2.2g_{m2}(C_L/C_c)$ if all other roots are $\geq 10GB$.

$$\text{Positive ICMR } V_{in(max)} = V_{DD} - \sqrt{\frac{I_5}{b_3}} - |V_{T03}|_{(max)} + V_{T1(min)}$$

$$\text{Negative ICMR } V_{in(min)} = V_{SS} + \sqrt{\frac{I_5}{b_1}} + V_{T1(max)} + V_{DS5(sat)}$$

Unbuffered Op Amp Design Procedure

This design procedure assumes that the gain at dc (A_v), unity gain bandwidth (GB), input common mode range ($V_{in}(\min)$ and $V_{in}(\max)$), load capacitance (C_L), slew rate (SR), settling time (T_s), output voltage swing ($V_{out}(\max)$ and $V_{out}(\min)$), and power dissipation (P_{diss}) are given. Choose the smallest device length which will keep the channel modulation parameter constant and give good matching for current mirrors.

1. From the desired phase margin, choose the minimum value for C_c , i.e. for a 60° phase margin we use the following relationship. This assumes that $z \geq 10GB$.

$$C_c > 0.22C_L$$

2. Determine the minimum value for the “tail current” (I_5) from

$$I_5 = SR \cdot C_c$$

3. Design for S_3 from the maximum input voltage specification.

$$S_3 = \frac{I_5}{K_3[V_{DD} - V_{in}(\max) - |V_{T03}|(\max) + V_{T1}(\min)]^2}$$

4. Verify that the pole of M3 due to C_{gs3} and C_{gs4} ($= 0.67W_3L_3C_{ox}$) will not be dominant by assuming it to be greater than $10 GB$

$$\frac{gm3}{2C_{gs3}} > 10GB.$$

Unbuffered Op Amp Design Procedure - Continued

5. Design for S_1 (S_2) to achieve the desired GB .

$$g_{m1} = GB \cdot C_c \rightarrow S_2 = \frac{g_{m1}^2}{K_1 I_5}$$

6. Design for S_5 from the minimum input voltage. First calculate $V_{DS5}(\text{sat})$ then find S_5 .

$$V_{DS5}(\text{sat}) = V_{in}(\text{min}) - V_{SS} - \sqrt{\frac{I_5}{\beta_1}} - V_{T1}(\text{max}) \geq 100 \text{ mV} \rightarrow S_5 = \frac{2I_5}{K_5 [V_{DS5}(\text{sat})]^2}$$

7. Find S_6 by letting the second pole (p_2) be equal to 2.2 times GB and assuming that $V_{SG4} = V_{SG6}$.

$$g_{m6} = 2.2g_{m2}(C_L/C_c) \quad \text{and} \quad \frac{g_{m6}}{g_{m4}} = \frac{\sqrt{2K_P'S_6I_6}}{\sqrt{2K_P'S_4I_4}} = \sqrt{\frac{S_6I_6}{S_4I_4}} = \frac{S_6}{S_4} \rightarrow S_6 = \frac{g_{m6}}{g_{m4}}S_4$$

8. Calculate I_6 from

$$I_6 = \frac{g_{m6}^2}{2K_6S_6}$$

Check to make sure that S_6 satisfies the $V_{out}(\text{max})$ requirement and adjust as necessary.

9. Design S_7 to achieve the desired current ratios between I_5 and I_6 .

$$S_7 = (I_6/I_5)S_5 \quad (\text{Check the minimum output voltage requirements})$$

Unbuffered Op Amp Design Procedure - Continued

10. Check gain and power dissipation specifications.

$$A_v = \frac{2g_{m2}g_{m6}}{I_5(\lambda_2 + \lambda_4)I_6(\lambda_6 + \lambda_7)} \quad P_{diss} = (I_5 + I_6)(V_{DD} + |V_{SS}|)$$

11. If the gain specification is not met, then the currents, I_5 and I_6 , can be decreased or the W/L ratios of M2 and/or M6 increased. The previous calculations must be rechecked to insure that they are satisfied. If the power dissipation is too high, then one can only reduce the currents I_5 and I_6 . Reduction of currents will probably necessitate increase of some of the W/L ratios in order to satisfy input and output swings.

12. Simulate the circuit to check to see that all specifications are met.

Unbuffered Op Amp Design Summary

Step	Design Equations	Comments
1	Let $C_c \geq 0.2C_L$	PM = 60° and RHP Z=10GB
2	$I_5 \geq SR \cdot C_c$	Assumes SR limited by C_c
3	$\frac{W_3}{L_3} = \frac{W_4}{L_4} = \frac{I_5}{K'_3 [V_{DD} - V_{in}(\max) - V_{T3} + V_{T1}]^2}$	Maximum input common mode range
4	$g_{m1} = GB \cdot C_c \rightarrow \frac{W_1}{L_1} = \frac{W_2}{L_2} = \frac{g_{m1}^2}{K'_1 I_5}$	GB defines the W/L of M1 and M2
5	$\frac{W_5}{L_5} = \frac{2I_5}{K'_5 V_{DS5}(sat)^2}$	Minimum input common mode range
6	$\frac{W_6}{L_6} = \frac{g_{m6}}{g_{m4}} \frac{W_4}{L_4}$	DC balance conditions
7	$I_6 = \frac{g_{m6}^2}{2K'_6 (W_6/L_6)}$	PM = 60° and $p_2 = 2.2GB$ give $g_{m6} \approx 10g_{m1}$
8	$\frac{W_7}{L_7} = \max \left[\frac{I_6}{I_5} \frac{W_5}{L_5}, \frac{2I_7}{K'_7 V_{DS7}(sat)^2} \right]$	Determines the current in M7
9	Check gain and power dissipation and iterate if necessary	$A_v = \frac{2g_{m1}g_{m6}}{I_5(\lambda_2 + \lambda_4)I_6(\lambda_6 + \lambda_7)}$ and $P_{diss} = (I_5 + I_6)(V_{DD} + V_{SS})$

DESIGN EXAMPLE OF A TWO-STAGE OP AMP

Example 23-1 - Design of a Two-Stage Op Amp

If $K_N' = 120 \mu\text{A}/\text{V}^2$, $K_P' = 25 \mu\text{A}/\text{V}^2$, $V_{TN} = |V_{TP}| = 0.5 \pm 0.15\text{V}$, $\lambda_N = 0.06\text{V}^{-1}$, and $\lambda_P = 0.08\text{V}^{-1}$, design a two-stage, CMOS op amp that meets the following specifications. Assume the channel length is to be $0.5 \mu\text{m}$ and the load capacitor is $C_L = 10\text{pF}$.

$$A_V > 3000\text{V}/\text{V} \quad V_{DD} = 2.5\text{V} \quad GB = 5\text{MHz} \quad SR > 10\text{V}/\mu\text{s}$$

$$60^\circ \text{ phase margin} \quad 0.5\text{V} < V_{out \text{ range}} < 2\text{V} \quad I_{CMR} = 1.25\text{V to } 2\text{V} \quad P_{diss} \leq 2\text{mW}$$

Solution

1.) The first step is to calculate the minimum value of the compensation capacitor C_c ,

$$C_c > (2.2/10)(10 \text{ pF}) = 2.2 \text{ pF}$$

2.) Choose C_c as 3pF. Using the slew-rate specification and C_c calculate I_5 .

$$I_5 = (3 \times 10^{-12})(10 \times 10^6) = 30 \mu\text{A}$$

3.) Next calculate $(W/L)_3$ using ICMR requirements (use worst case thresholds $\pm 0.15\text{V}$).

$$(W/L)_3 = \frac{30 \times 10^{-6}}{(25 \times 10^{-6})[2.5 - 2 - .65 + 0.35]^2} = 30 \quad \rightarrow \quad \boxed{(W/L)_3 = (W/L)_4 = 30}$$

Example 23-1 - Continued

4.) Now we can check the value of the mirror pole, p_3 , to make sure that it is in fact greater than $10GB$. Assume the $C_{ox} = 6fF/\mu m^2$. The mirror pole can be found as

$$p_3 \approx \frac{-g_{m3}}{2C_{gs3}} = \frac{-\sqrt{2K'_p S_3 I_3}}{2(0.667)W_3 L_3 C_{ox}} = -1.25 \times 10^9 (\text{rads/sec})$$

or 199 MHz. Thus, p_3 , is not of concern in this design because $p_3 \gg 10GB$.

5.) The next step in the design is to calculate g_{m1} to get

$$g_{m1} = (5 \times 10^6)(2\pi)(3 \times 10^{-12}) = 94.25 \mu S$$

Therefore, $(W/L)_1$ is

$$(W/L)_1 = (W/L)_2 = \frac{g_{m1}^2}{2K'_N I_1} = \frac{(94.25)^2}{2 \cdot 120 \cdot 15} = 2.47 \approx 3.0 \Rightarrow \boxed{(W/L)_1 = (W/L)_2 = 3}$$

6.) Next calculate V_{DS5} ,

$$V_{DS5} = 1.25 - \sqrt{\frac{30 \times 10^{-6}}{120 \times 10^{-6} \cdot 3}} - .65 = 0.31V$$

Using V_{DS5} calculate $(W/L)_5$ from the saturation relationship.

$$(W/L)_5 = \frac{2(30 \times 10^{-6})}{(120 \times 10^{-6})(0.31)^2} = 5.16 \approx 6 \quad \rightarrow \quad \boxed{(W/L)_5 = 6}$$

Example 23-1 - Continued

7.) For 60° phase margin, we know that

$$g_{m6} \geq 10g_{m1} \geq 942.5\mu\text{S}$$

Assuming that $g_{m6} = 942.5\mu\text{S}$ and knowing that $g_{m4} = 150\mu\text{S}$, we calculate $(W/L)_6$ as

$$(W/L)_6 = 30 \frac{942.5 \times 10^{-6}}{(150 \times 10^{-6})} = 188.5 \approx 190 \quad \boxed{(W/L)_6 = 190}$$

8.) Calculate I_6 using the small-signal g_m expression:

$$I_6 = \frac{(942.5 \times 10^{-6})^2}{(2)(25 \times 10^{-6})(188.5)} = 94.2\mu\text{A} \approx 95\mu\text{A}$$

Calculating $(W/L)_6$ based on $V_{out}(\text{max})$, gives a value of 15. Since 190 exceeds the specification and gives better phase margin, we choose $(W/L)_6 = 190$ and $I_6 = 95\mu\text{A}$.

With $I_6 = 95\mu\text{A}$ the power dissipation is $P_{diss} = 2.5\text{V} \cdot (30\mu\text{A} + 95\mu\text{A}) = 0.3125\text{mW}$

9.) Finally, calculate $(W/L)_7$

$$(W/L)_7 = 6 \left(\frac{95 \times 10^{-6}}{30 \times 10^{-6}} \right) = 19 \approx 20 \quad \rightarrow \quad \boxed{(W/L)_7 = 20}$$

Let us check the $V_{out}(\text{min})$ specification although the W/L of M7 is so large that this is probably not necessary. The value of $V_{out}(\text{min})$ is

$$V_{out}(\text{min}) = V_{DS7}(\text{sat}) = \sqrt{(2 \cdot 95)/(120 \cdot 20)} = 0.281\text{V}$$

which is less than required. At this point, the first-cut design is complete.