## Example 23-1 - Continued

10.) Now check to see that the gain specification has been met

$$A_v = \frac{(94.25 \text{x} 10^{-6})(942.5 \text{x} 10^{-6})}{15 \text{x} 10^{-6}(.06 + .08)95 \text{x} 10^{-6}(.06 + .08)} = 3{,}180 \text{V/V}$$

which barely exceeds the specifications. Since we are at $2 \text{x} L_{min}$, it won't do any good to increase the channel lengths. Decreasing the currents or increasing W_6/L_6 will help.

The figure below shows the results of the first-cut design. The W/L ratios shown do not account for the lateral diffusion discussed above. The next phase requires simulation.
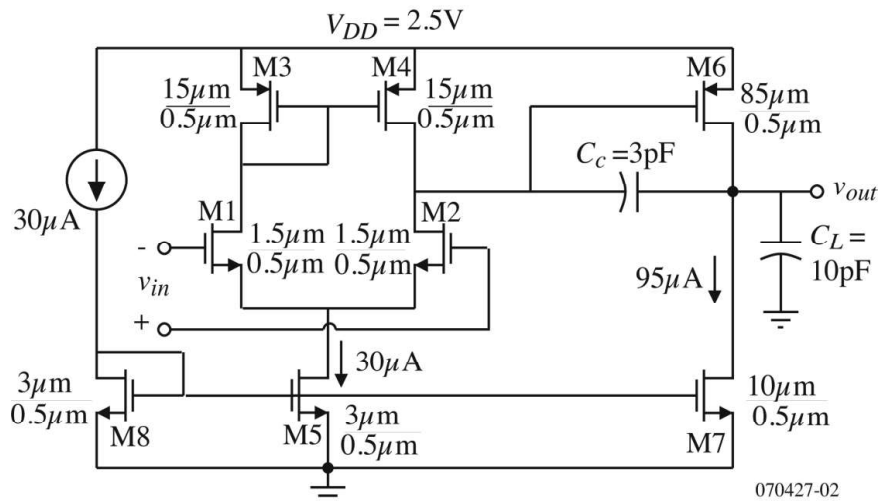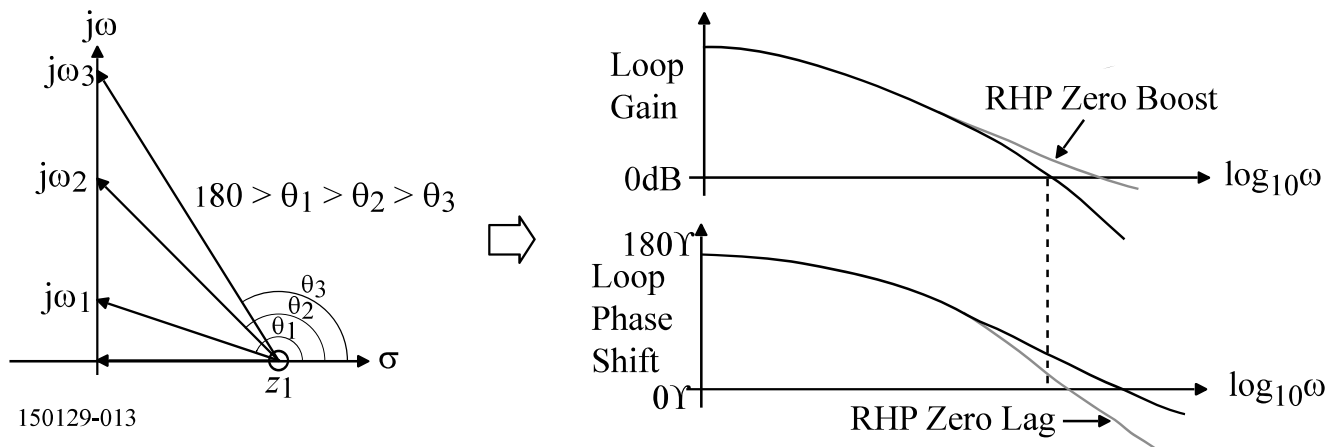
RIGHT-HALF PLANE ZERO

Controlling the Right-Half Plane Zero

Why is the RHP zero a problem?

Because it boosts the magnitude but lags the phase - the worst possible combination for stability.

150129-013

Solution of the problem:

The compensation comes from the *feedback path* through C_c, but the RHP zero comes from the *feedforward path* through C_c so <u>eliminate the feedforward path</u>!

Elimination of the Feedforward Path through the Miller Capacitor

1.) Removing the feedforward path.

Roots: Dominant pole and output pole.

Feedback Only
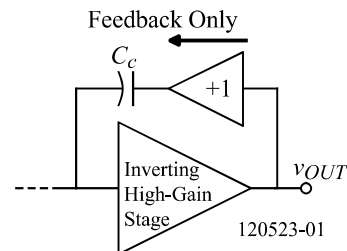
2.) Controlling the RHP zero location using a nulling resistor[†].
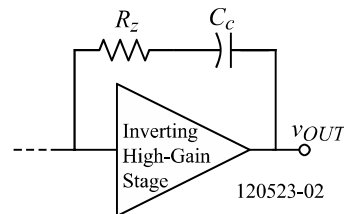
Roots:

a.) Dominant pole (Miller pole)

b.) Output pole

c.) Pole due to R_z and first stage output capacitance, $p_4 \approx \dfrac{-1}{R_z C_I}$

d.) Controllable zero, $z_1 = \dfrac{1}{C_c(1/g_{mII} - R_z)}$

Note that z_1 can be placed anywhere on the real axis.

[†] W.J. Parrish, "An Ion Implanted CMOS Amplifier for High Performance Active Filters", Ph.D. Dissertation, 1976, Univ. of CA, Santa Barbara.

A Design Procedure that Allows the RHP Zero to Cancel the Output Pole, p_2

We desire that $z_1 = p_2$ in terms of the previous notation.

Therefore,

$$\frac{1}{C_c(1/g_{mII} - R_z)} = \frac{-g_{mII}}{C_{II}}$$

The value of R_z can be found as

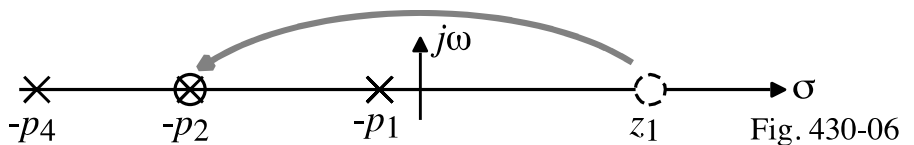$$R_z = \left(\frac{C_c + C_{II}}{C_c}\right)(1/g_{mII})$$

Fig. 430-06

With p_2 canceled, the remaining roots are p_1 and p_4(the pole due to R_z) . For unity-gain stability, all that is required is that

$$|p_4| > A_v(0)|p_1| = \frac{A_v(0)}{g_{mII}R_{II}R_IC_c} = \frac{g_{mI}}{C_c} \qquad \text{and} \qquad (1/R_zC_I) > (g_{mI}/C_c) = GB$$

Substituting R_z into the above inequality and assuming $C_{II} >> C_c$ results in
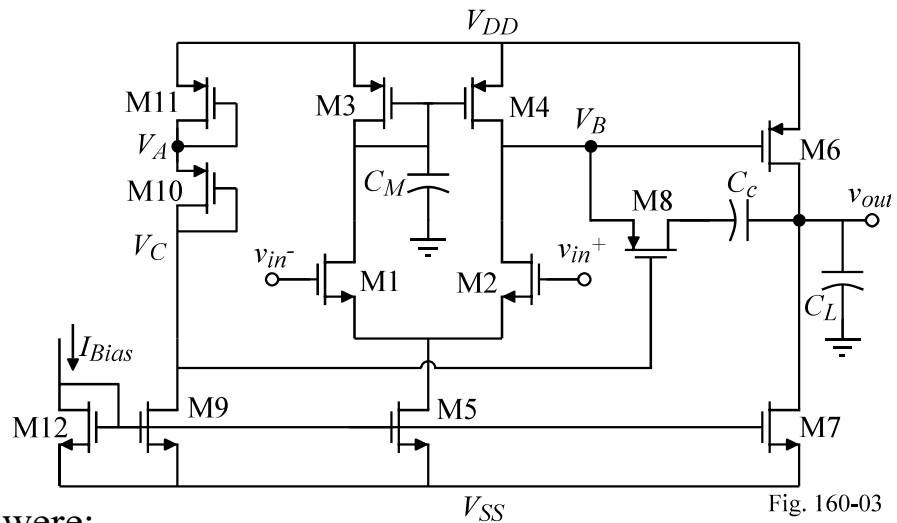
$$C_c > \sqrt{\frac{g_{mI}}{g_{mII}}C_IC_{II}}$$

This procedure gives excellent stability for a fixed value of C_{II} ($\approx C_L$).

Unfortunately, as C_L changes, p_2 changes and the zero must be readjusted to cancel p_2.

Using the Nulling Resistor in the Miller Compensated Two-Stage Op Amp

Circuit:

Fig. 160-03

We saw earlier that the roots were:

$$p_1 = -\frac{g_{m2}}{A_v C_c} = -\frac{g_{m1}}{A_v C_c} \qquad\qquad p_2 = -\frac{g_{m6}}{C_L}$$

$$p_4 = -\frac{1}{R_z C_I} \qquad\qquad z_1 = \frac{-1}{R_z C_c - C_c/g_{m6}}$$

where $A_v = g_{m1}g_{m6}R_I R_{II}$.

(Note that p_4 is the pole resulting from the nulling resistor compensation technique.)

Design of the Nulling Resistor (M8)

For the zero to be on top of the second pole (p_2), the following relationship must hold

$$R_z = \frac{1}{g_{m6}}\left(\frac{C_L + C_c}{C_c}\right) = \left(\frac{C_c + C_L}{C_c}\right)\frac{1}{\sqrt{2K'_P S_6 I_6}}$$

The resistor, R_z, is realized by the transistor M8 which is operating in the active region because the dc current through it is zero. Therefore, R_z, can be written as

$$R_z = \frac{v_{DS8}}{i_{D8}}\bigg|_{V_{DS8}=0} = \frac{1}{K'_P S_8 (V_{SG8} - |V_{TP}|)}$$

The bias circuit is designed so that voltage V_A is equal to V_B.

$$\therefore \quad |V_{GS10}| - |V_T| = |V_{GS8}| - |V_T| \Rightarrow \quad V_{SG11} = V_{SG6} \quad\quad \Rightarrow \quad \left(\frac{W_{11}}{L_{11}}\right) = \left(\frac{I_{10}}{I_6}\right)\left(\frac{W_6}{L_6}\right)$$

In the saturation region

$$|V_{GS10}| - |V_T| = \sqrt{\frac{2(I_{10})}{K'_P(W_{10}/L_{10})}} = |V_{GS8}| - |V_T|$$

$$\therefore \quad R_z = \frac{1}{K'_P S_8}\sqrt{\frac{K'_P S_{10}}{2I_{10}}} = \frac{1}{S_8}\sqrt{\frac{S_{10}}{2K'_P I_{10}}}$$

Equating the two expressions for R_z gives $\quad \left(\frac{W_8}{L_8}\right) = \left(\frac{C_c}{C_L + C_c}\right)\sqrt{\frac{S_{10}S_6 I_6}{I_{10}}}$

Example 23-2 - RHP Zero Compensation

Use results of Ex. 23-1 and design compensation circuitry so that the RHP zero is moved from the RHP to the LHP and placed on top of the output pole p_2. Use device data given in Ex. 23-1.

Solution

The task at hand is the design of transistors M8, M9, M10, M11, and bias current I_{10}. The first step in this design is to establish the bias components. In order to set V_A equal to V_B, then V_{SG11} must equal V_{SG6}. Therefore,
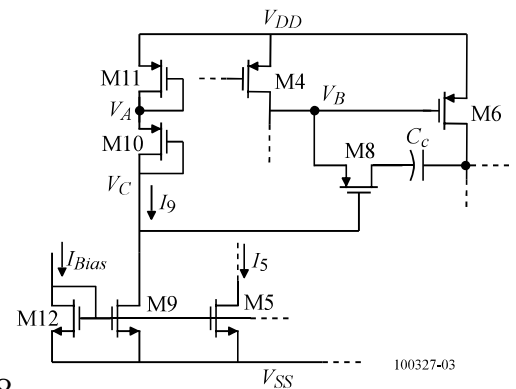
$$S_{11} = (I_{11}/I_6)S_6$$

Choose $I_{11} = I_{10} = I_9 = 15\mu A$ which gives $S_{11} = (15\mu A/95\mu A)190 = 30$.

The aspect ratio of M10 is essentially a free parameter, and will be set equal to 1. There must be sufficient supply voltage to support the sum of V_{SG11}, V_{SG10}, and V_{DS9}. The ratio of I_{10}/I_5 determines the (W/L) of M9. This ratio is

$$(W/L)_9 = (I_{10}/I_5)(W/L)_5 = (15/30)(6) = 3$$

Now $(W/L)_8$ is determined to be

$$(W/L)_8 = \left(\frac{3pF}{3pF+10pF}\right)\sqrt{\frac{1\cdot190\cdot95\mu A}{15\mu A}} = 8$$

Example 23-2 - Continued

It is worthwhile to check that the RHP zero has been moved on top of p_2. To do this, first calculate the value of R_z. V_{SG8} must first be determined. It is equal to V_{SG10}, which is

$$V_{SG10} = \sqrt{\frac{2I_{10}}{K'_P S_{10}}} + |V_{TP}| = \sqrt{\frac{2 \cdot 15}{25 \cdot 1}} + 0.5 = 1.595V$$

Next determine R_z.

$$R_z = \frac{1}{K'_P S_8 (V_{SG10} - |V_{TP}|)} = \frac{10^6}{25 \cdot 8(1.595 - .7)} = 4.564k\Omega$$

The location of z_1 is calculated as

$$z_1 = \frac{-1}{(4.564 \times 10^3)(3 \times 10^{-12}) - \dfrac{3 \times 10^{-12}}{950 \times 10^{-6}}} = -94.91 \times 10^6 \text{ rads/sec}$$

The output pole, p_2, is

$$p_2 = -\frac{950 \times 10^{-6}}{10 \times 10^{-12}} = -95 \times 10^6 \text{ rads/sec}$$

Thus, we see that for all practical purposes, the output pole is canceled by the zero that has been moved from the RHP to the LHP.

The results of this design are summarized below where $L = 0.5\mu m$.

$W_8 = 4\mu m$ $W_9 = 1.5\mu m$ $W_{10} = 0.5\mu m$ and $W_{11} = 15 \ \mu m$

An Alternate Form of Nulling Resistor

To cancel p_2,

$$z_1 = p_2 \rightarrow R_z = \frac{C_c + C_L}{g_{m6A}C_C} = \frac{1}{g_{m6B}}$$

Which gives

$$g_{m6B} = g_{m6A}\left(\frac{C_c}{C_c + C_L}\right)$$

In the previous example,

$$g_{m6A} = 950\mu S, \; C_c = 3pF$$

and $C_L = 10pF$.

Choose $I_{6B} = 10\mu A$ to get

$$g_{m6B} = \frac{g_{m6A}C_c}{C_c + C_L} \rightarrow \sqrt{\frac{2K_P W_{6B} I_{6B}}{L_{6B}}} = \left(\frac{C_c}{C_c + C_L}\right)\sqrt{\frac{2K_P W_{6A} I_{D6}}{L_{6A}}}$$

or

$$\frac{W_{6B}}{L_{6B}} = \left(\frac{3}{13}\right)^2 \frac{I_{6A}}{I_{6B}}\frac{W_{6A}}{L_{6A}} = \left(\frac{3}{13}\right)^2\left(\frac{95}{10}\right)(190) = 96.12 \rightarrow W_{6B} = 48\mu m$$

Fig. 6.3-4A

CMOS Analog Circuit Design   © P.E. Allen - 2016
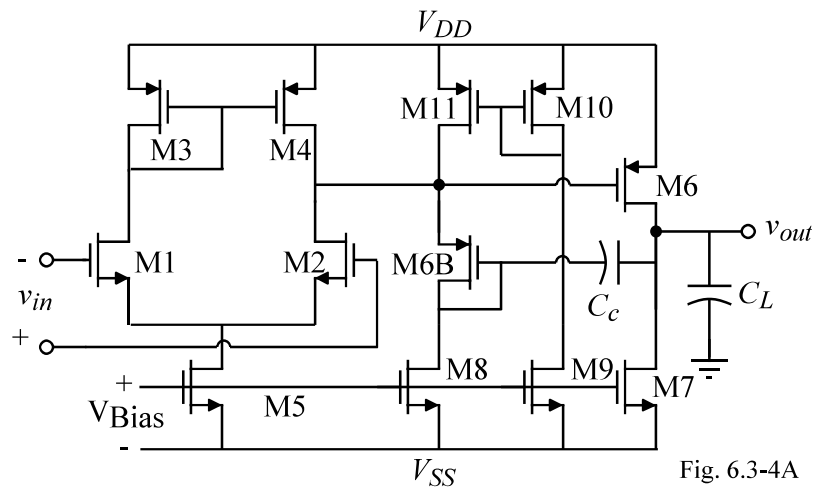
Increasing the Magnitude of the Output Pole[†]

The magnitude of the output pole, p_2, can be increased by introducing gain in the Miller capacitor feedback path as shown where,

$$A \approx g_{m8}(r_{ds8}\|r_{ds9}\|r_{ds2}\|r_{ds4}).$$
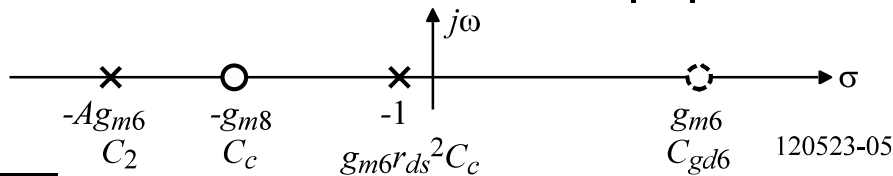
The roots become,

1.) The dominant pole increased slightly because R_I (output of first stage) is decreased.
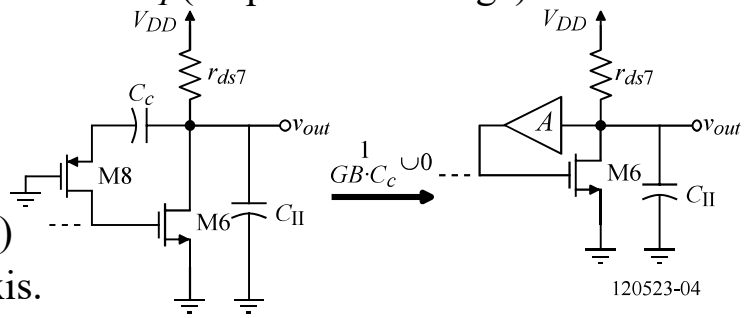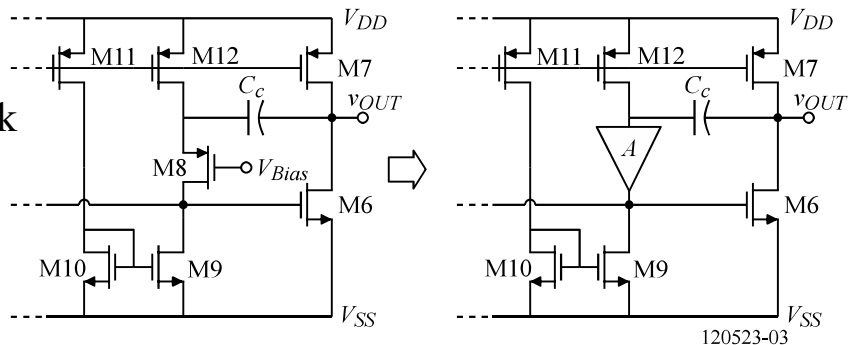
2.) The output pole is increased by a

factor of A to get new $p_2 \approx \dfrac{-Ag_{m6}}{C_{II}}$

3.) The pole at the source of M8 ($-g_{m8}/C_c$) becomes a zero on the negative real axis.

Roots:

$$-\dfrac{Ag_{m6}}{C_2} \qquad -\dfrac{g_{m8}}{C_c} \qquad \dfrac{-1}{g_{m6}r_{ds}{}^2C_c} \qquad \dfrac{g_{m6}}{C_{gd6}}$$

120523-05

† B.K. Ahuja, "An Improved Frequency Compensation Technique for CMOS Operational Amplifiers," *IEEE J. of Solid-State Circuits*, Vol. SC-18, No. 6 (Dec. 1983) pp. 629-633.

Issues with the Previous Method[†]

The previous technique assumed that the gate-source capacitance of M8 could be neglected. Unfortunately, this assumption ignores a pair of complex poles near the unity gain frequency. Below is the small signal model with the capacitance that causes this that includes C_{gs8}.
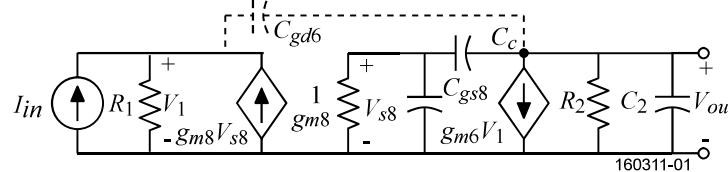
The solution proposed in the reference below is to decrease the impedance at the source of M8 by using a negative feedback loop. Below is a possible solution that will have better phase margin.
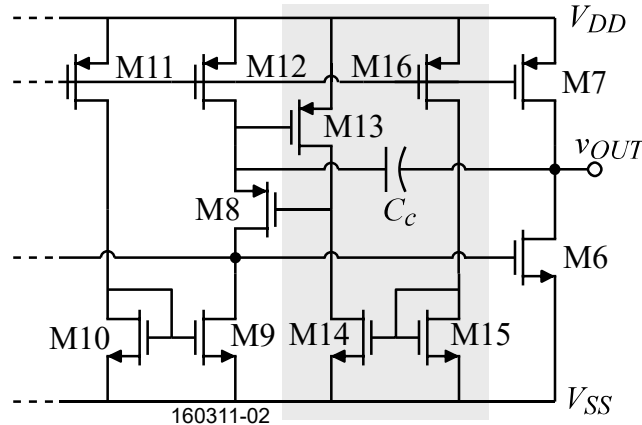
[†] Uday Dasgupta, "Issues with 'Ahuja' Frequency Compensation Technique," Proc. of IEEE Inter. Symposium on Radio Frequency Integration Technology, Jan. 9, 2009, pp. 326-329.

POWER SUPPLY REJECTION RATIO OF THE TWO-STAGE OP AMP

What is *PSRR*?

$$PSRR = \frac{A_v(V_{dd}=0)}{A_{dd}(V_{in}=0)}$$

How do you calculate *PSRR*?

You could calculate A_v and A_{dd} and divide, however
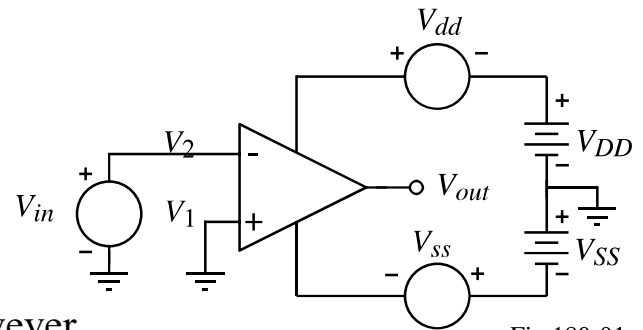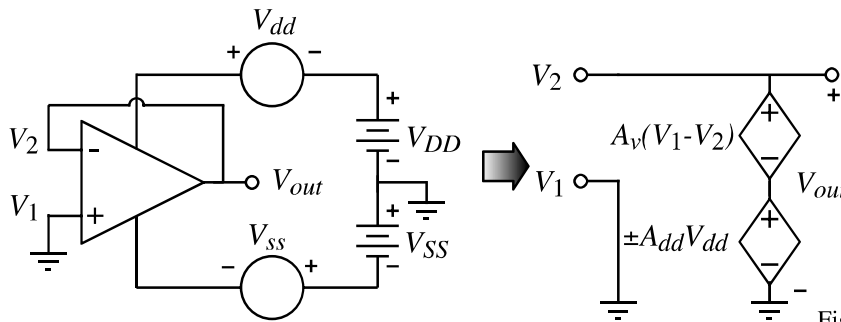
Fig.180-01

$V_{out} = A_{dd}V_{dd} + A_v(V_1-V_2) = A_{dd}V_{dd} - A_vV_{out}$ → $V_{out}(1+A_v) = A_{dd}V_{dd}$

$$\therefore \qquad \frac{V_{out}}{V_{dd}} = \frac{A_{dd}}{1+A_v} \approx \frac{A_{dd}}{A_v} = \frac{1}{PSRR^+} \qquad \text{(Good for frequencies up to } GB\text{)}$$
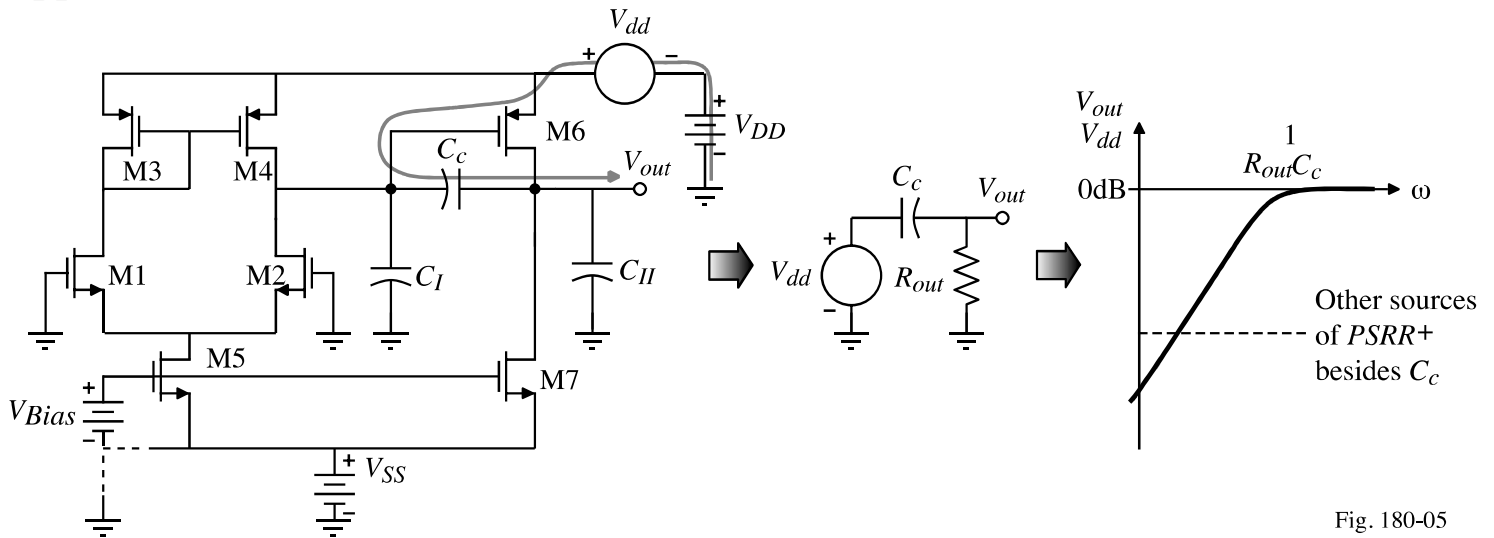
Fig. 180-02

Approximate Model for *PSRR*$^+$

Fig. 180-05

1.) The M7 current sink causes V_{SG6} to act like a battery.

2.) Therefore, V_{dd} couples from the source to gate of M6.

3.) The path to the output is through any capacitance from gate to drain of M6.

Conclusion:

The Miller capacitor C_c couples the positive power supply ripple directly to the output.

Must reduce or eliminate C_c.
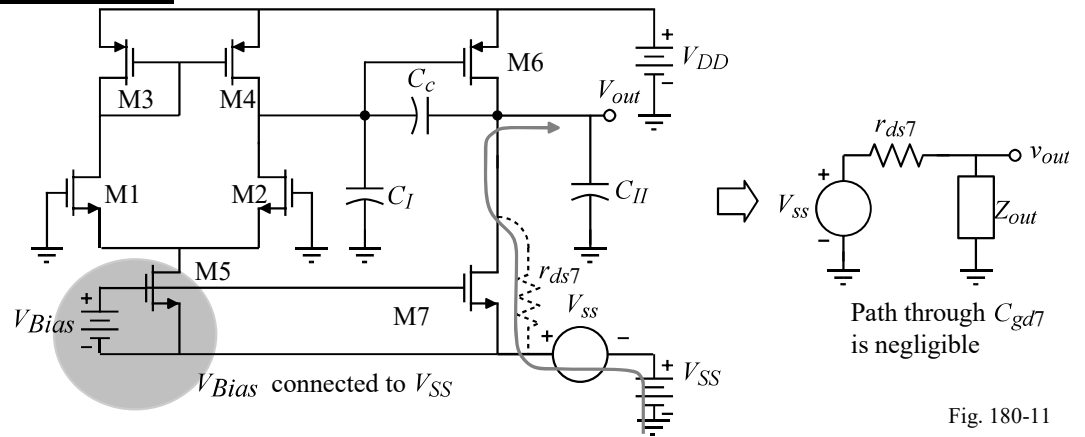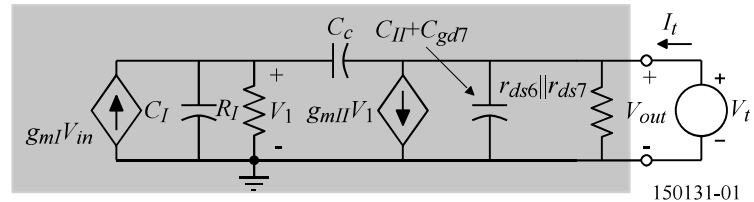
Approximate Model for *PSRR⁻*

Fig. 180-11

Path through C_{gd7} is negligible

What is Z_{out}?

$$Z_{out} = \frac{V_t}{I_t} \Rightarrow I_t = g_{mII}V_1 = g_{mII}\left(\frac{g_{mI}V_t}{G_I + sC_I + sC_c}\right)$$

Thus, $Z_{out} = \dfrac{G_I + s(C_I + C_c)}{g_{mI}g_{MII}}$

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$$\therefore \frac{V_{out}}{V_{SS}} = \frac{1 + \dfrac{r_{ds7}}{Z_{out}}}{1} = \frac{s(C_c + C_I) + G_I + g_{mI}g_{mII}r_{ds7}}{s(C_c + C_I) + G_I} \quad \Rightarrow \quad \text{Pole at } \frac{-G_I}{C_c + C_I}$$

The negative *PSRR* is much better than the positive *PSRR*.

SUMMARY

- The output of the design of an op amp is

    - Schematic

    - DC currents

    - W/L ratios

    - Component values

- Design procedures provide an organized approach to creating the dc currents, W/L ratios, and the component values

- The right-half plane zero causes the Miller compensation to deteriorate

- Methods for eliminating the influence of the RHP zero are:

    - Nulling resistor

    - Increasing the magnitude of the output pole

- The $PSRR$ of the two-stage op amp is poor because of the Miller capacitance, however, methods exist to eliminate this problem

- The two-stage op amp is a very general and flexible op amp