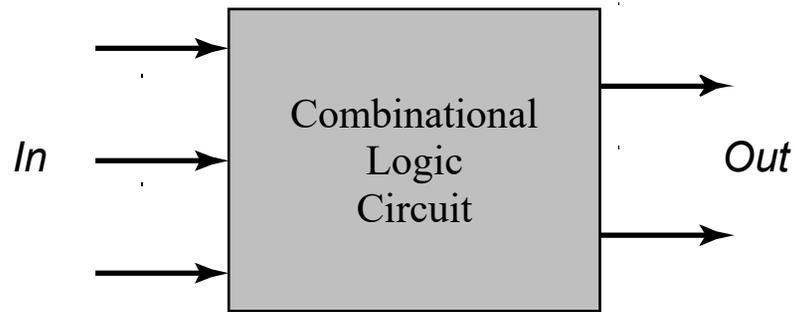
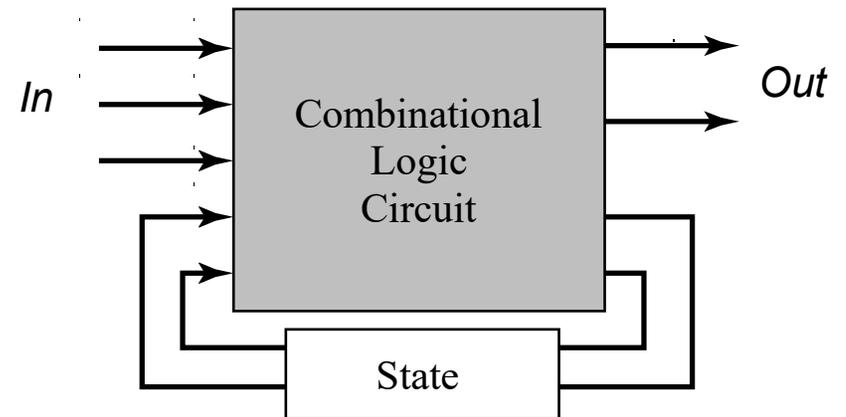


Combinational vs. Sequential Logic



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$$\text{Output} = f(\text{In})$$



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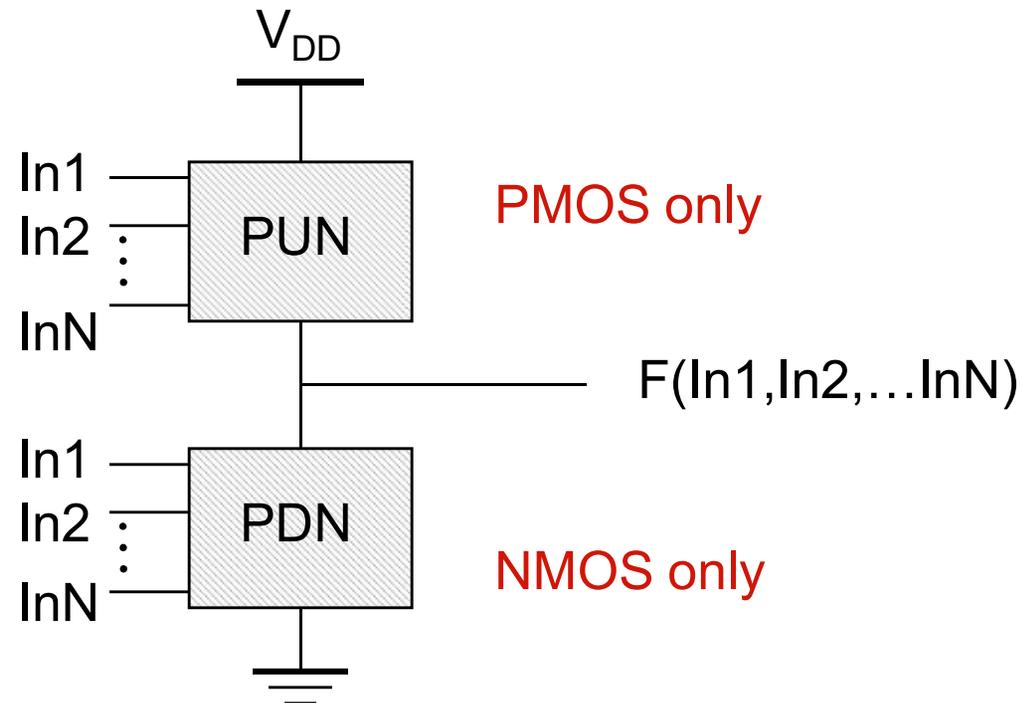
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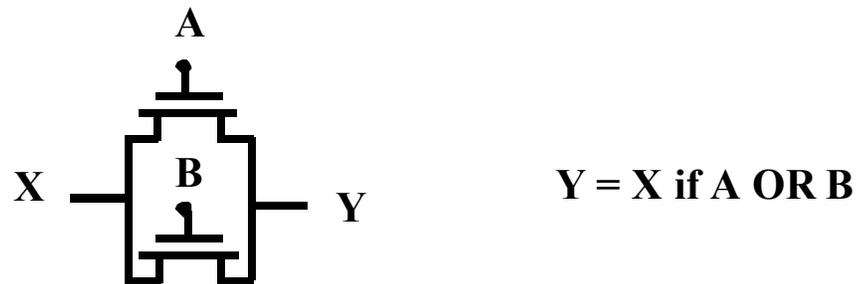
Static Complementary CMOS



PUN and PDN are **dual** logic networks

NMOS Transistors in Series/Parallel Connection

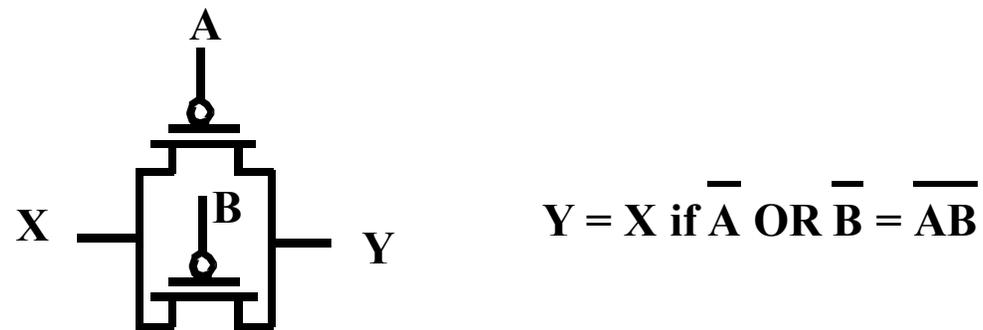
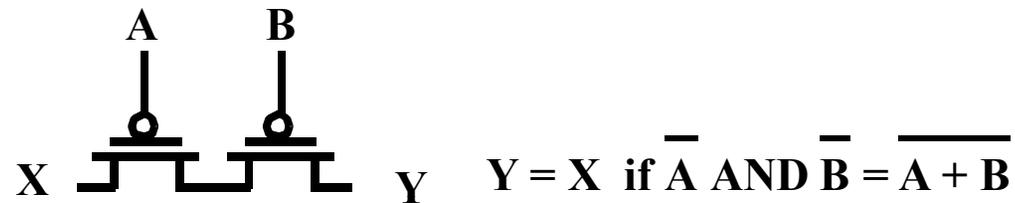
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NMOS Transistors pass a “strong” 0 but a “weak” 1

PMOS Transistors in Series/Parallel Connection

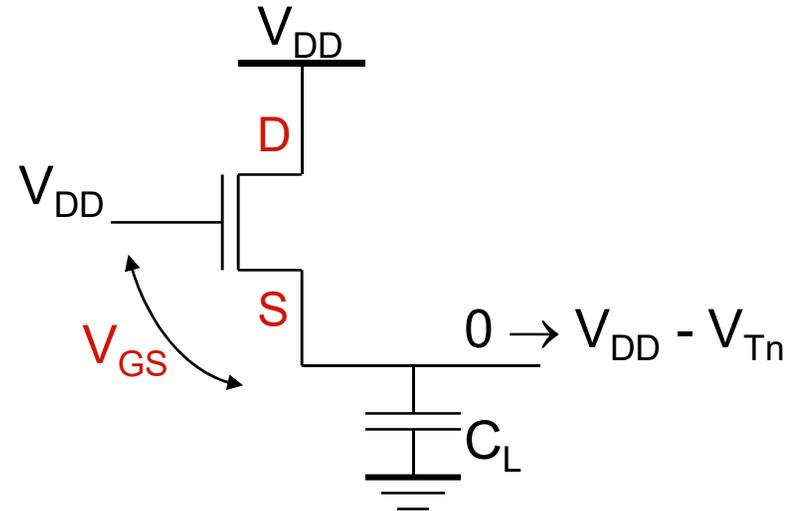
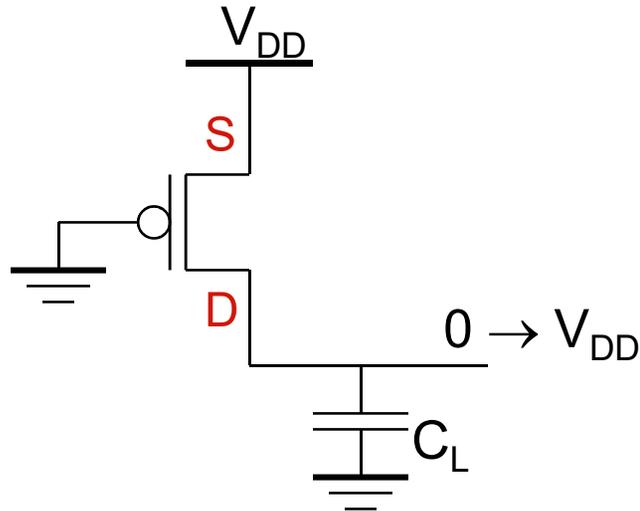
PMOS switch closes when switch control input is low



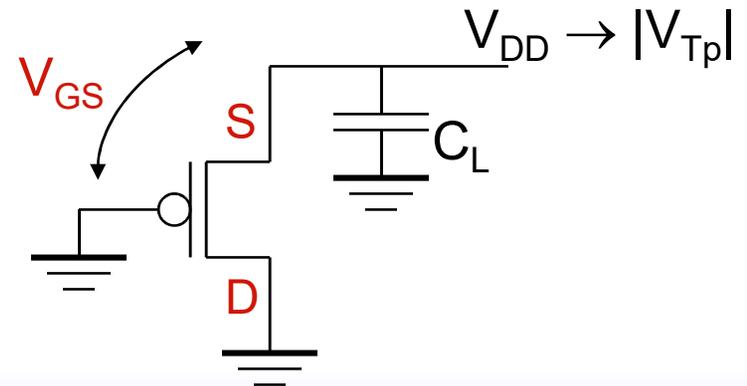
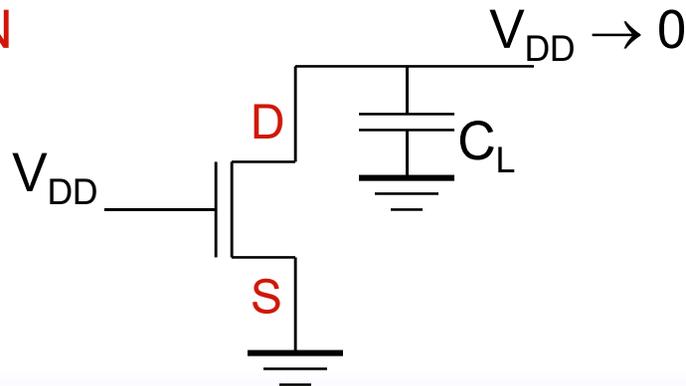
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Threshold Drops

PUN



PDN



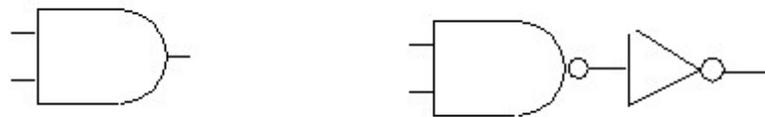
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$$\overline{A + B} = \bar{A}\bar{B}$$

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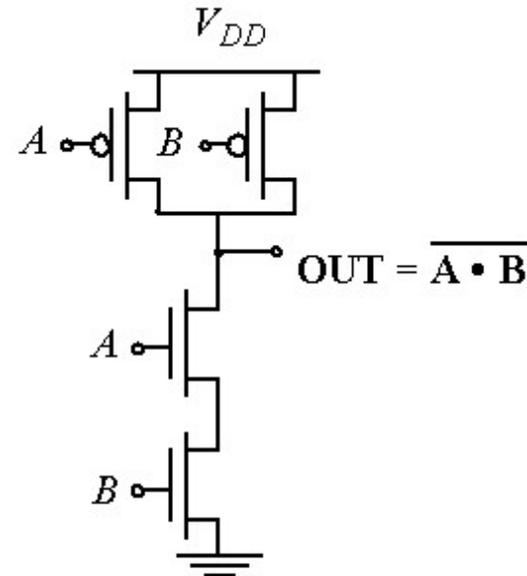


AND = NAND + INV

Example Gate: NAND

A	B	Out
0	0	1
0	1	1
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1	1	0

Truth Table of a 2 input NAND gate



PDN: $G = A B \Rightarrow$ Conduction to GND

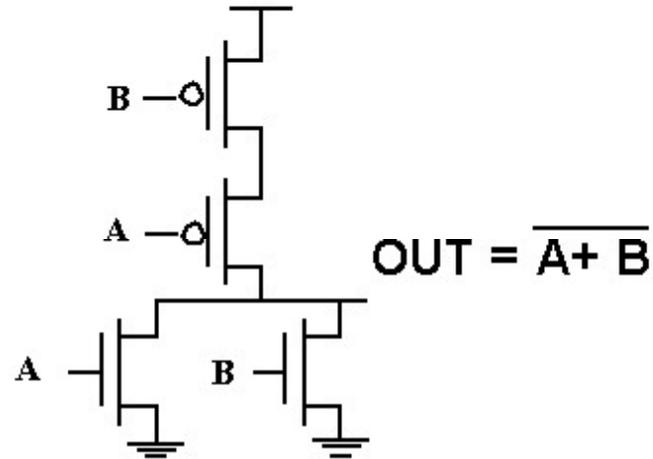
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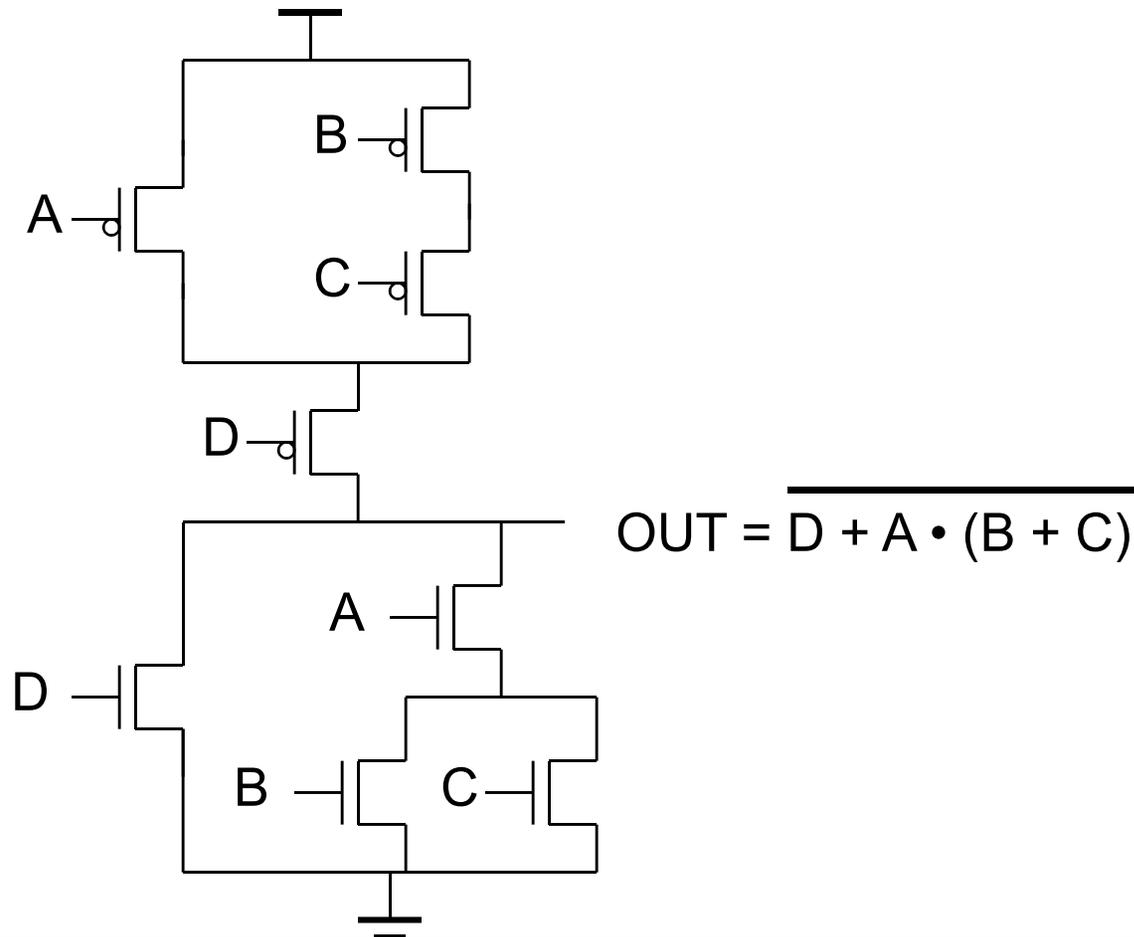
Example Gate: NOR

A	B	Out
0	0	1
0	1	0
1	0	0
1	1	0

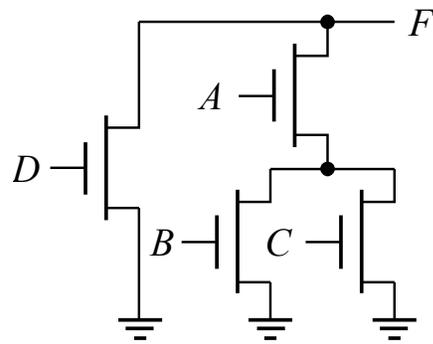
Truth Table of a 2 input NOR gate



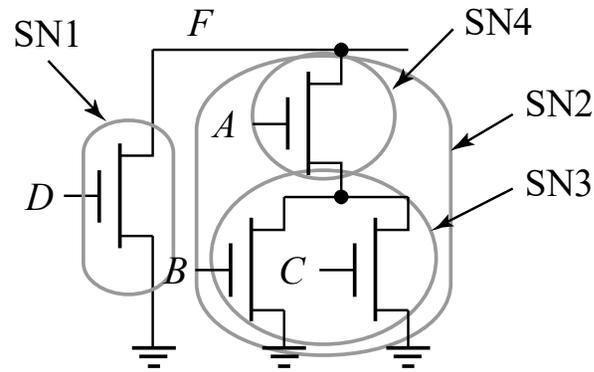
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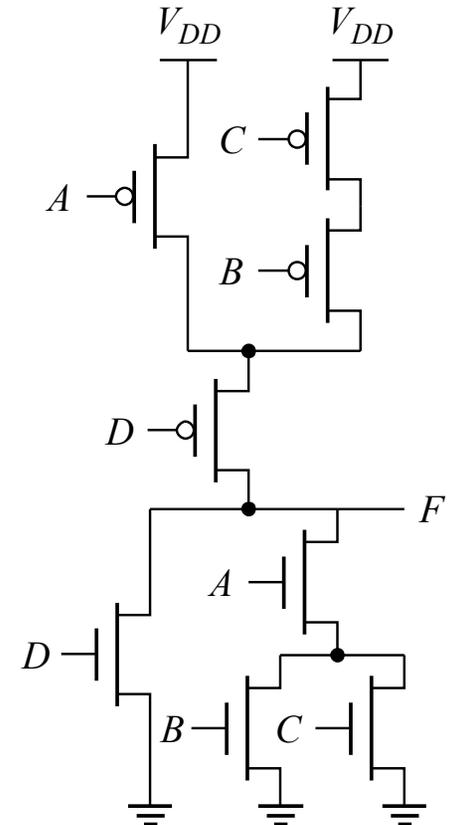
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(a) pull-down network



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Cell Design

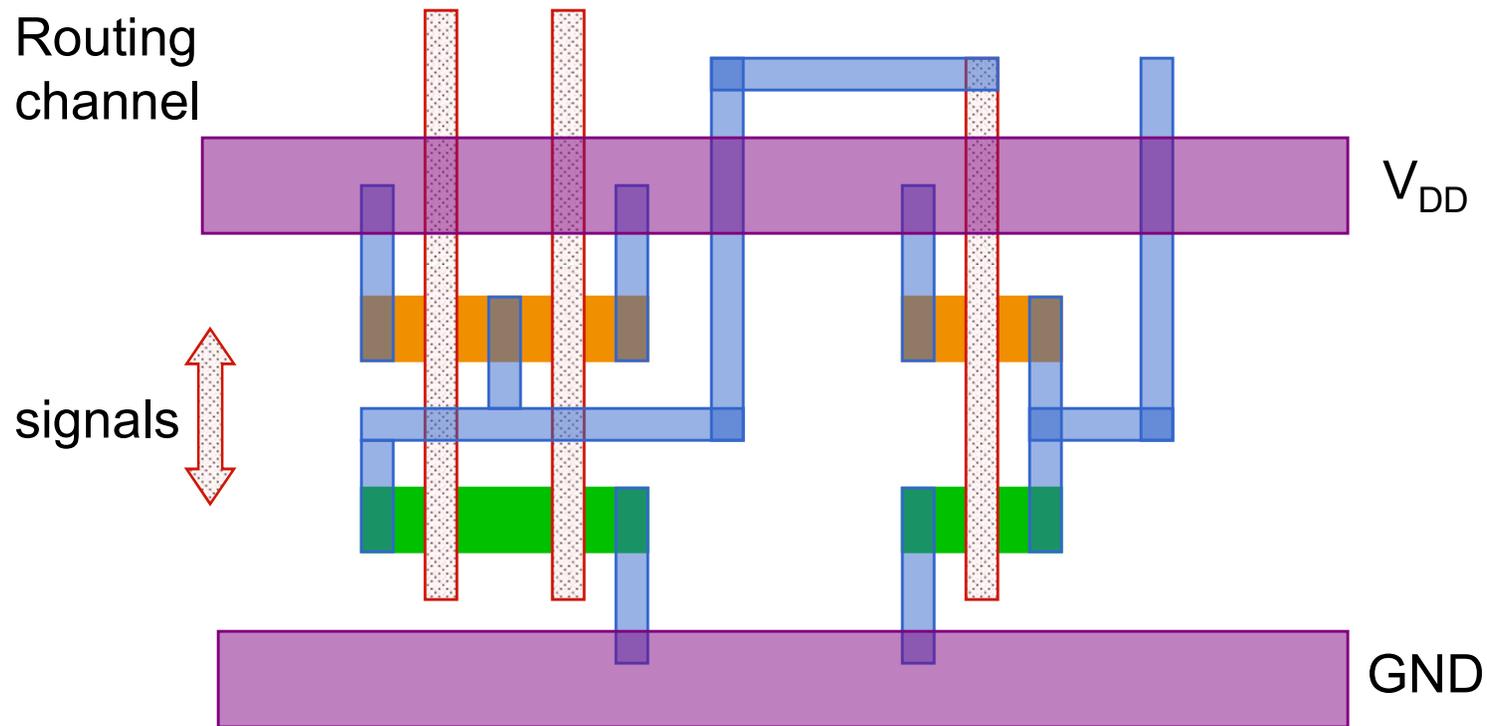
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- Can be synthesized
- Same height, varying width

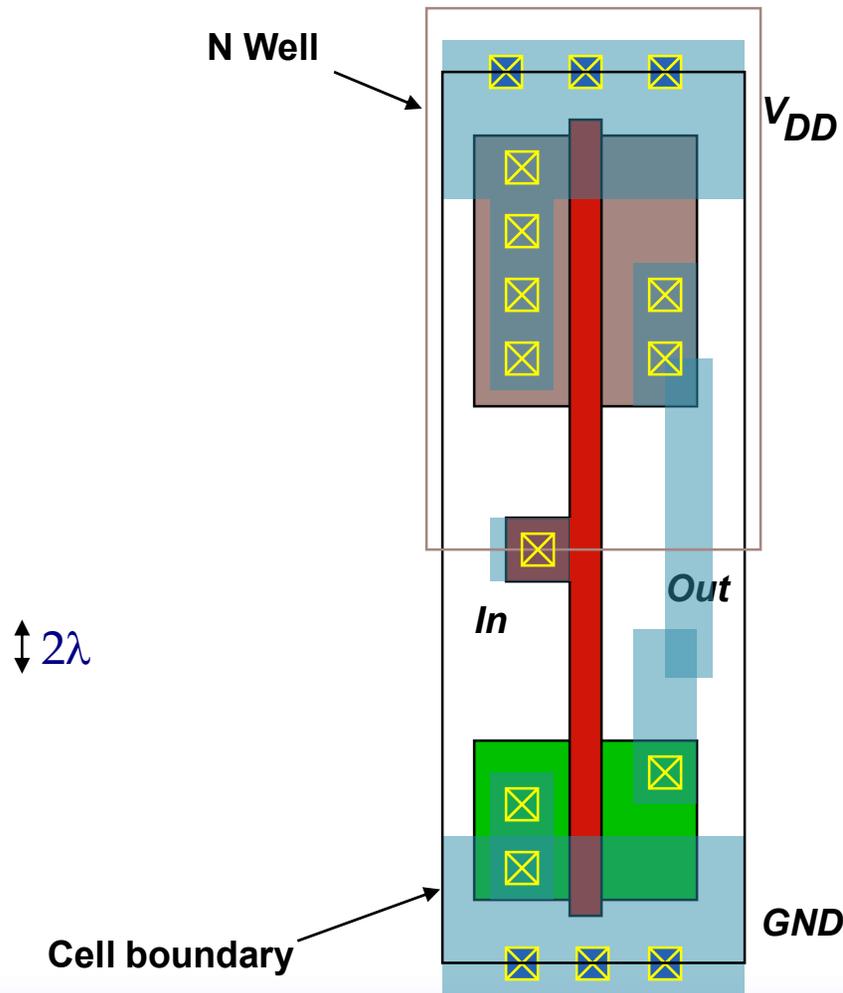
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Standard Cell Layout Methodology – 1980s



Standard Cells

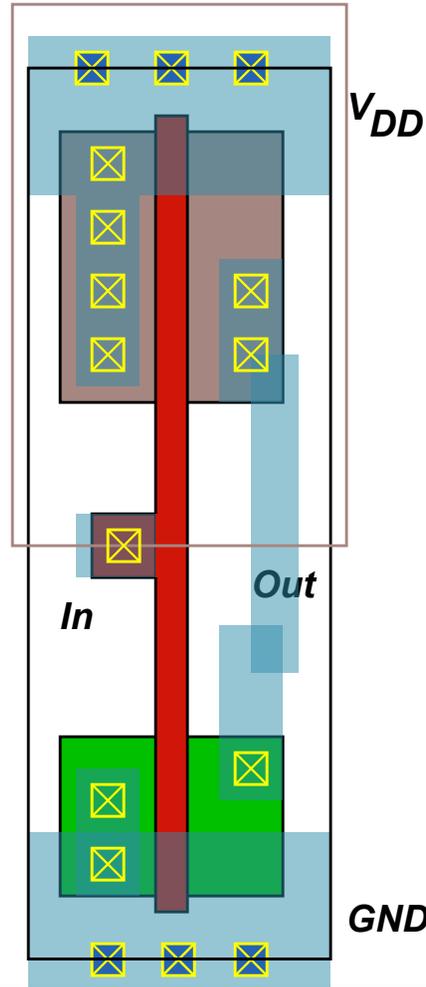
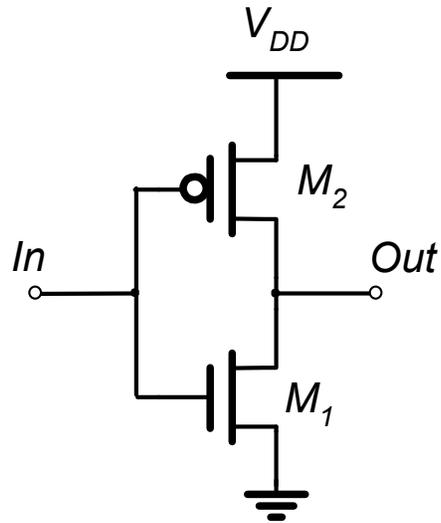


Cell height 12 metal tracks
Metal track is approx. $3\lambda + 3\lambda$
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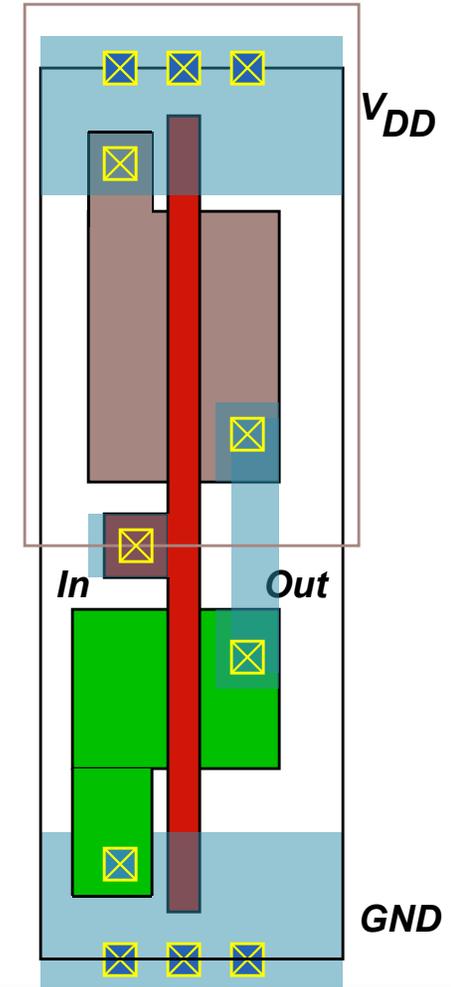
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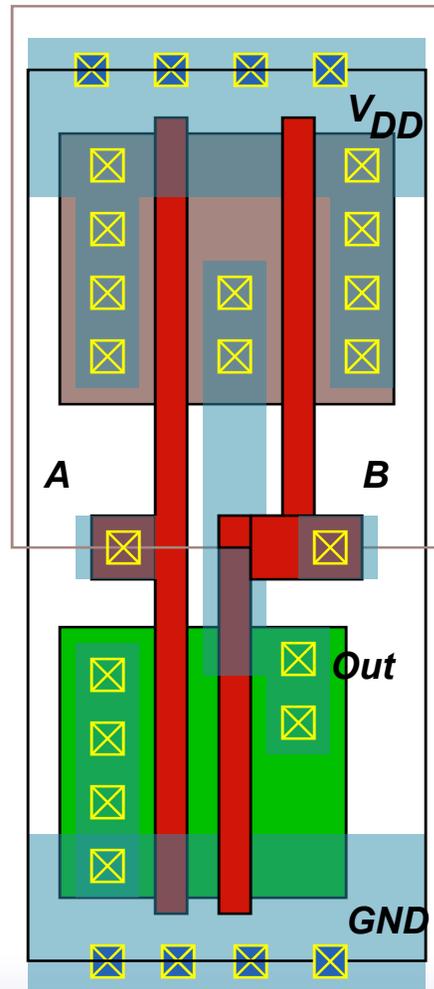
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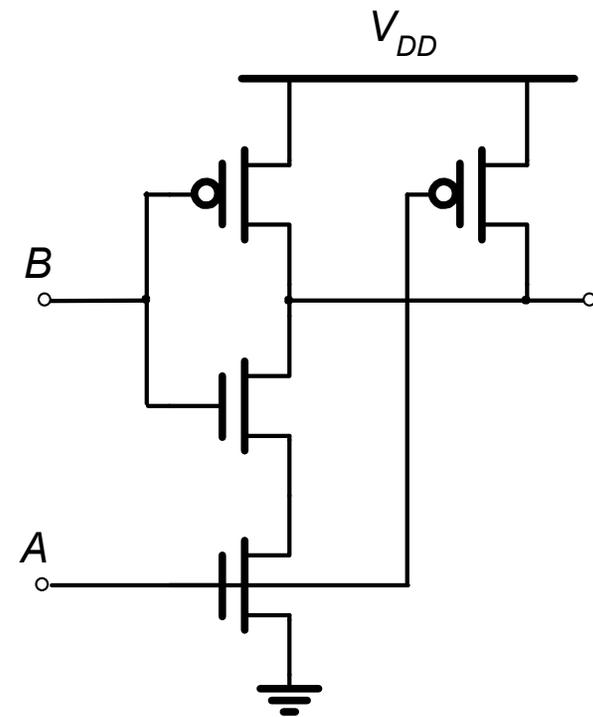
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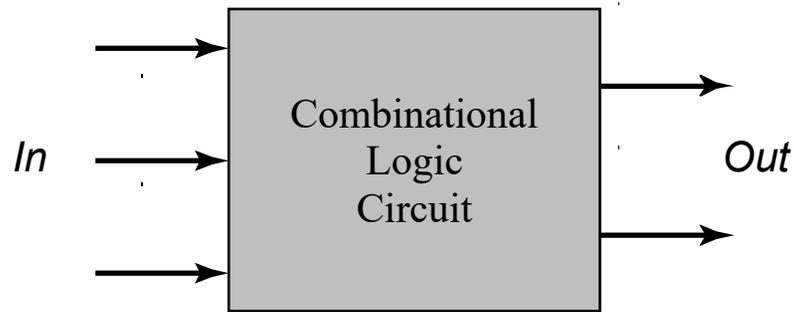
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2-input NAND gate

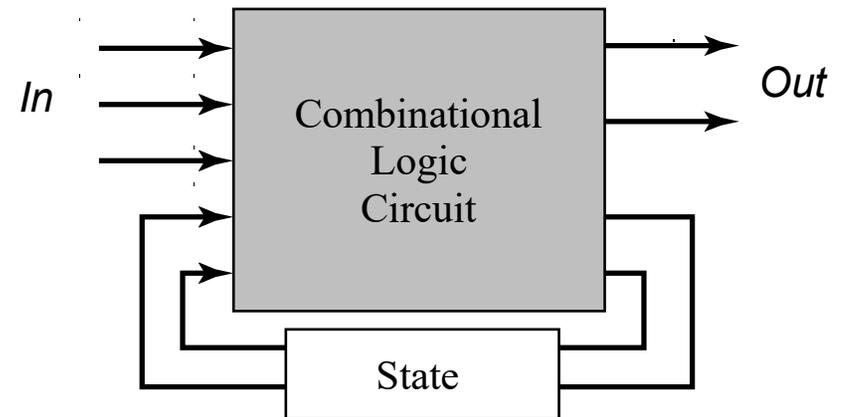


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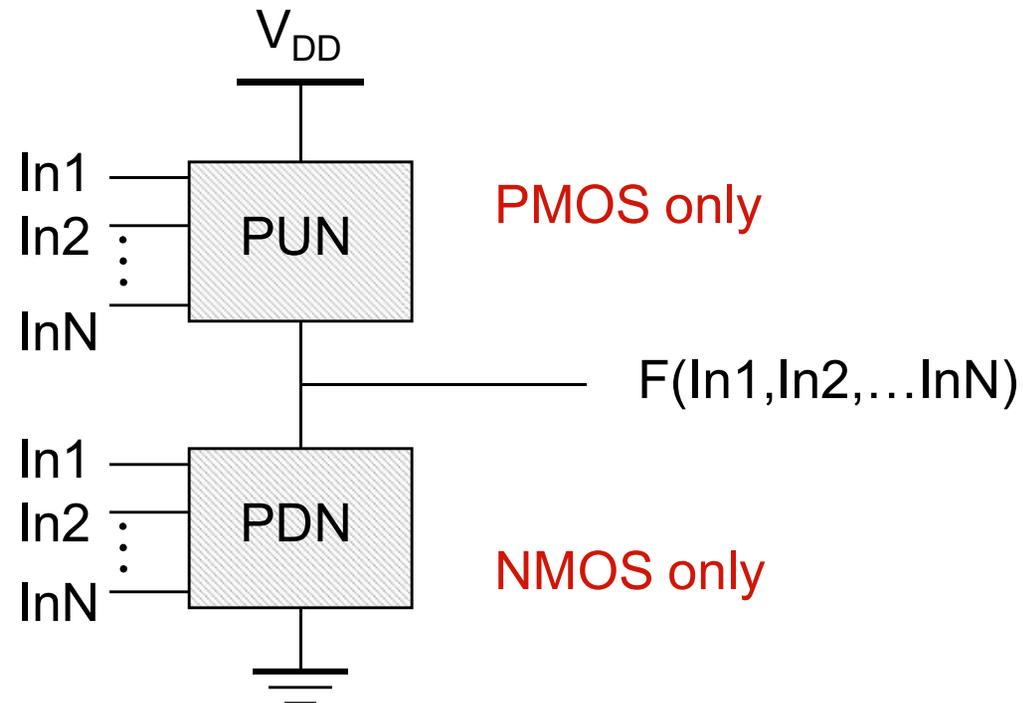
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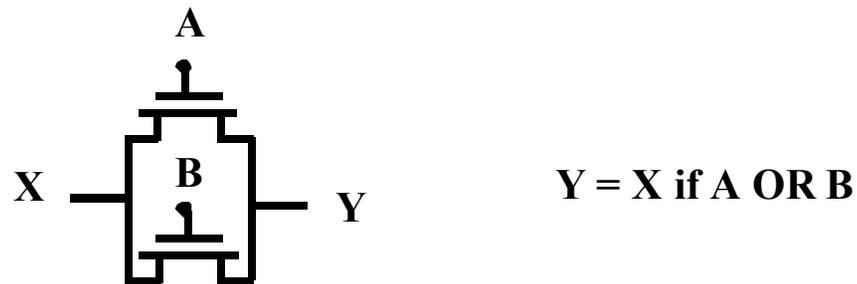
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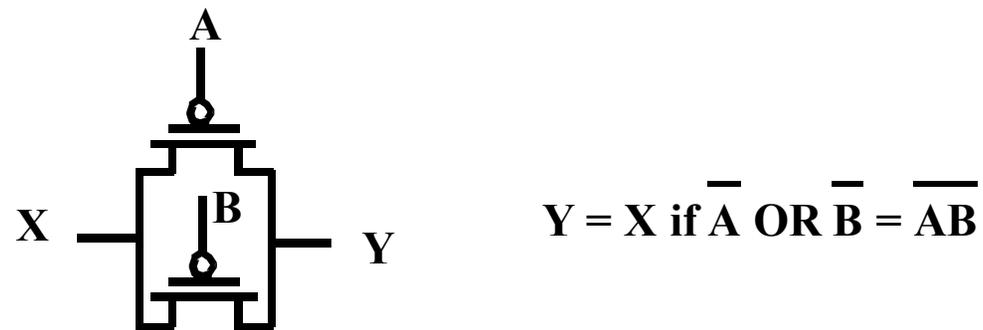
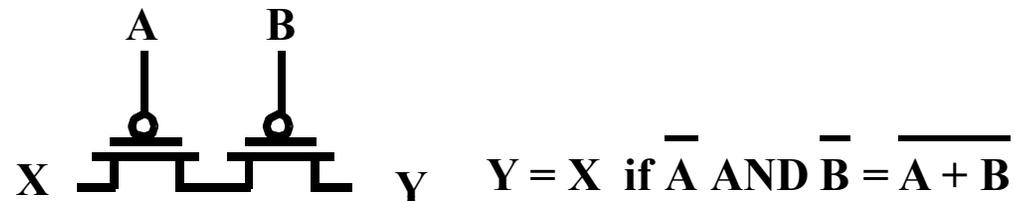
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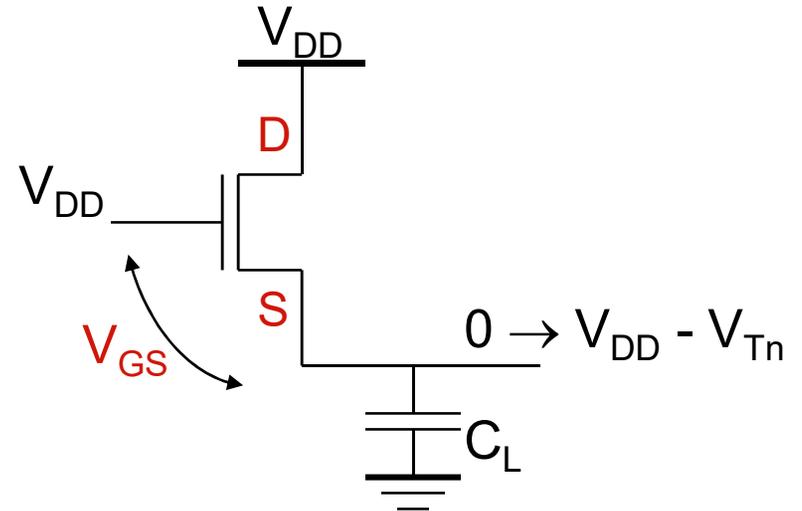
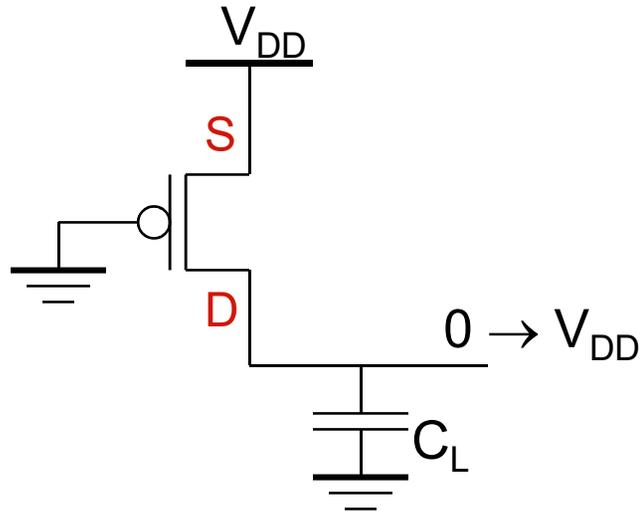
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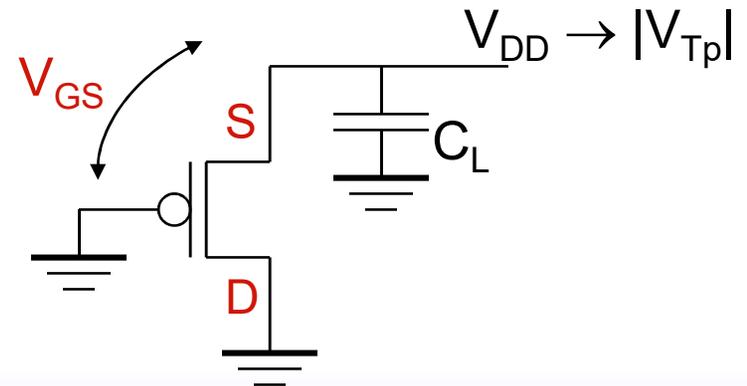
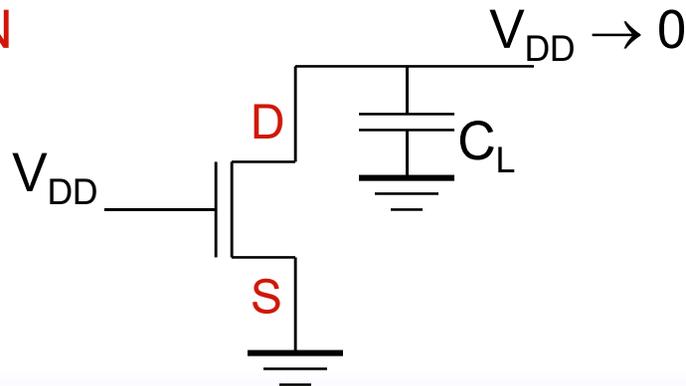
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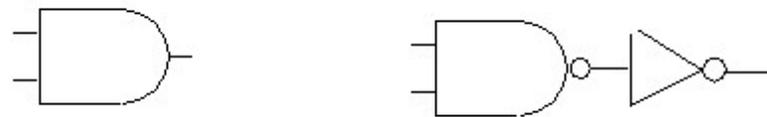
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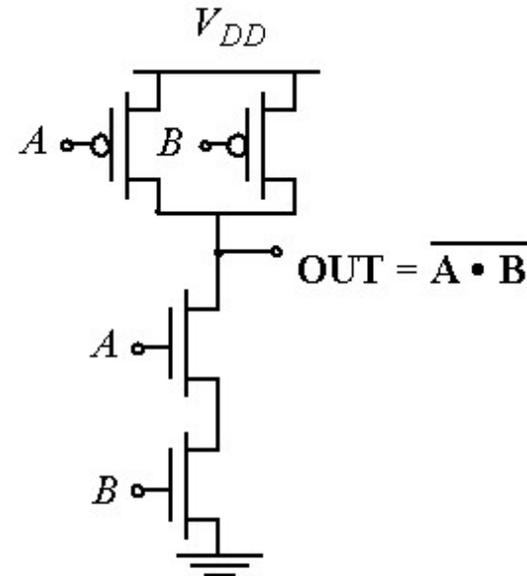


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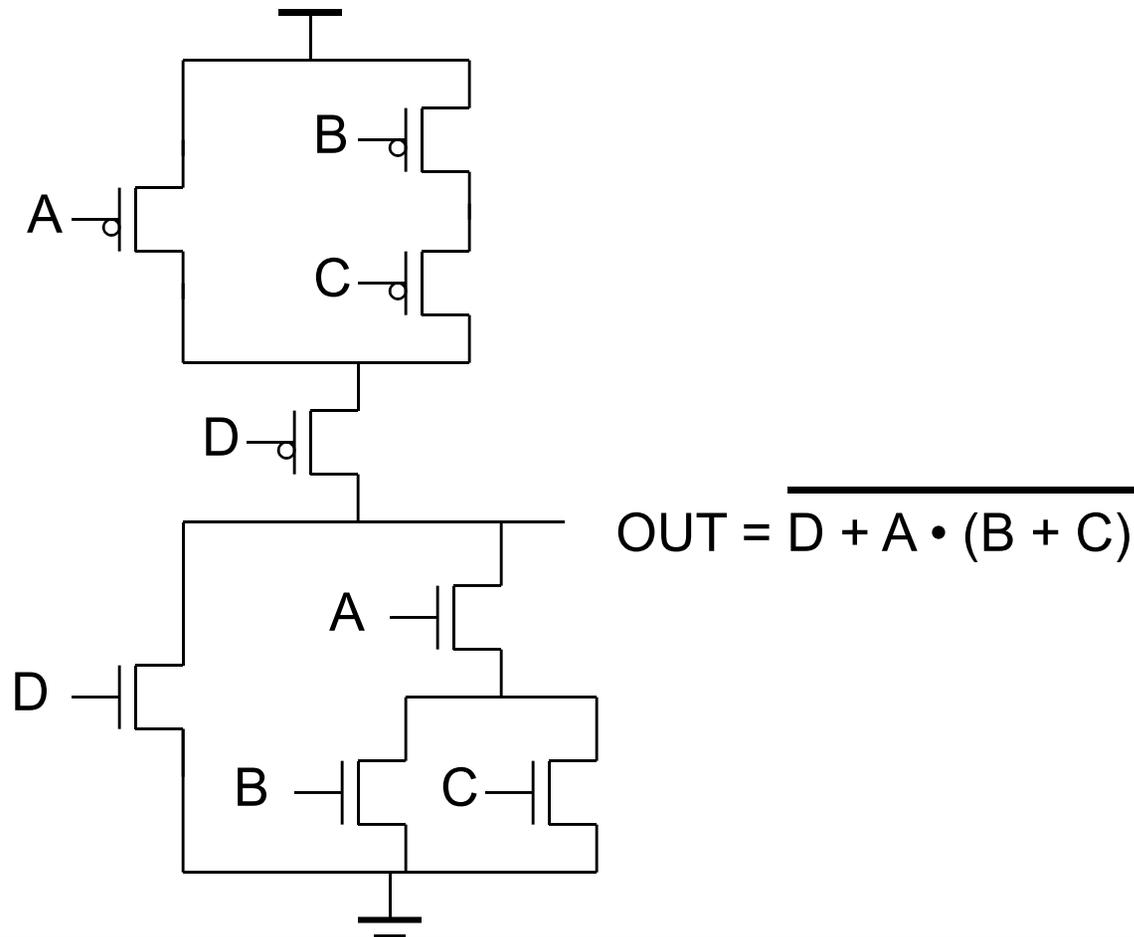


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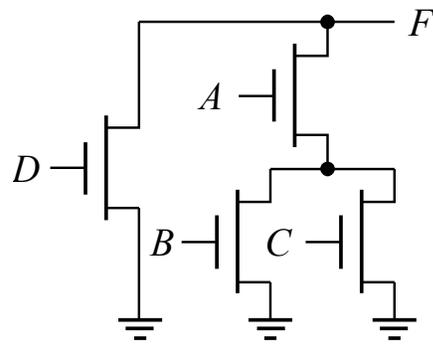
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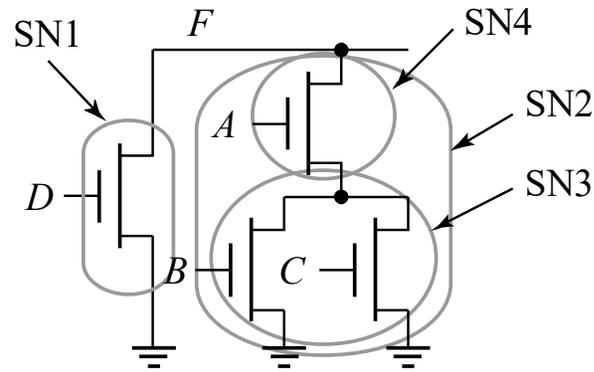
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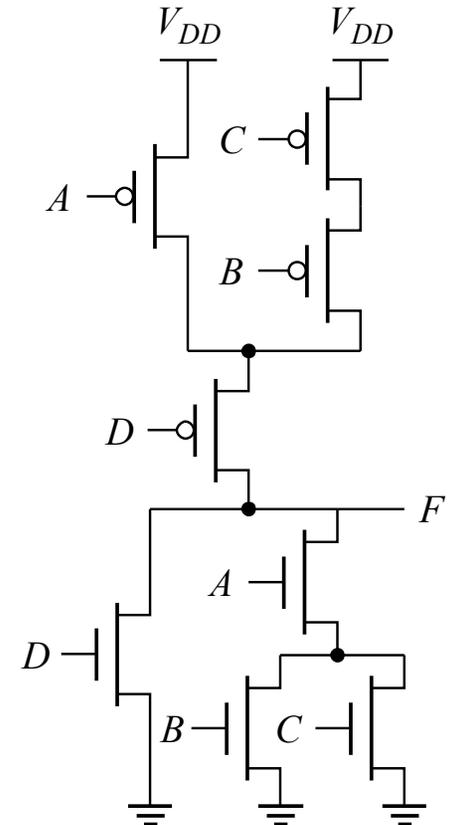
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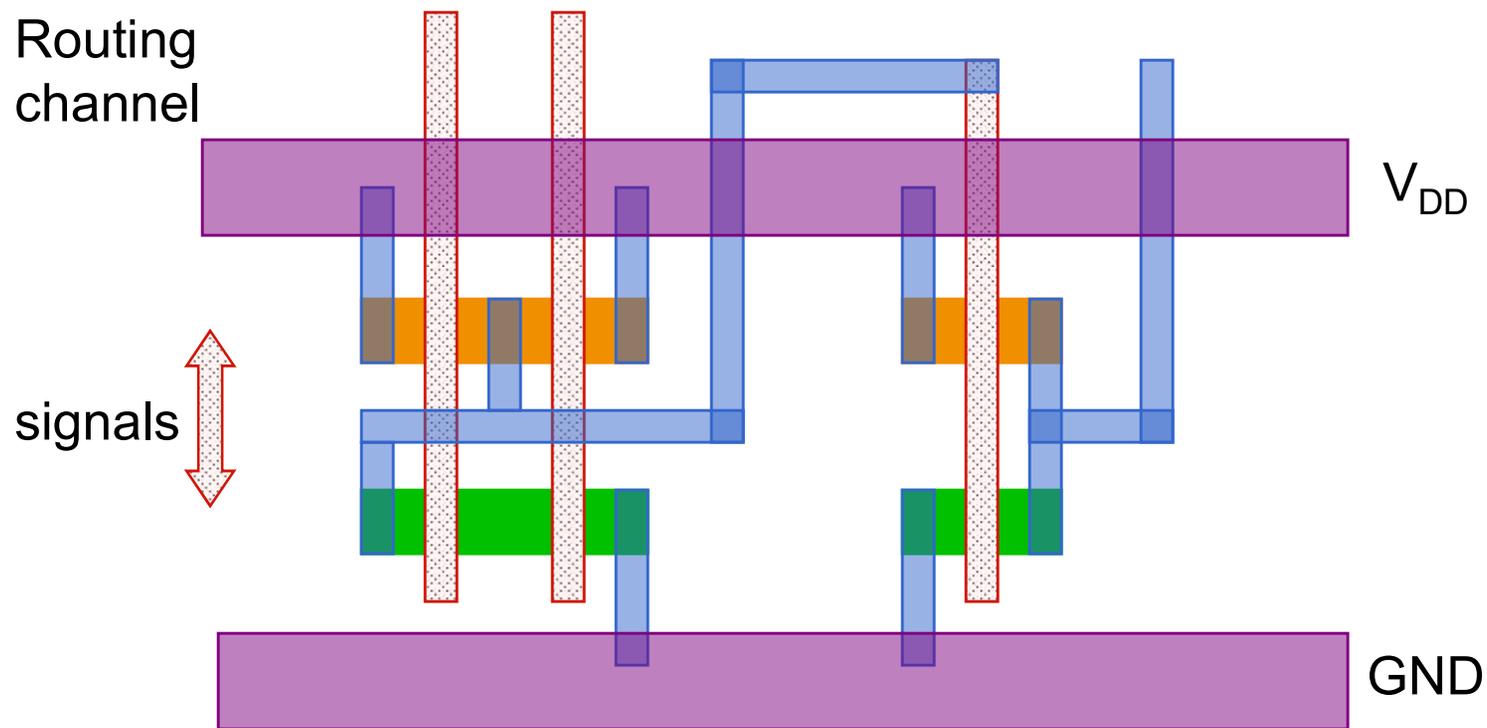
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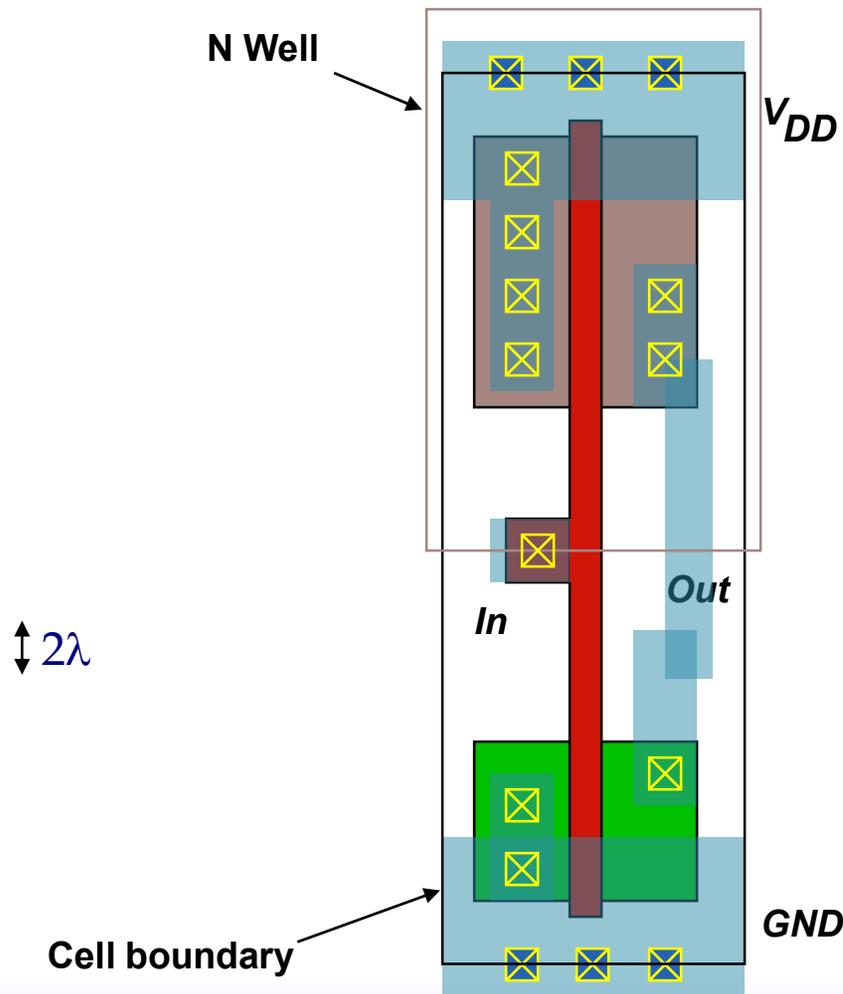
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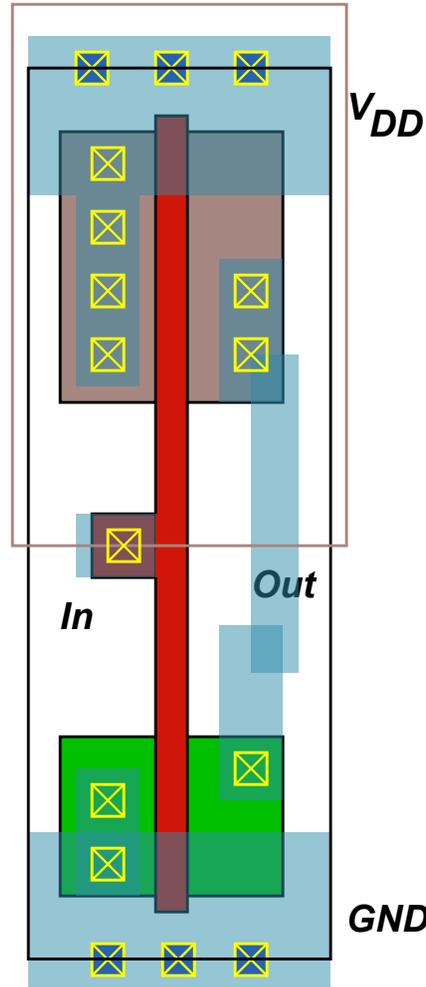
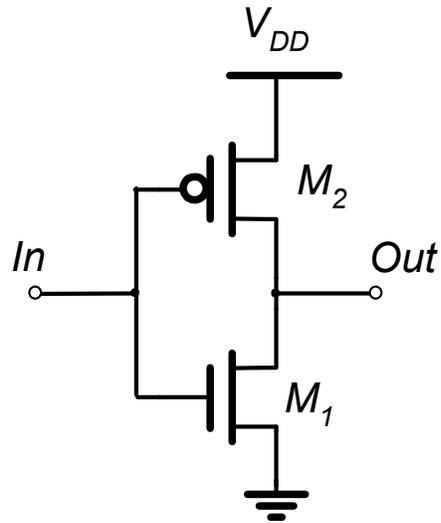
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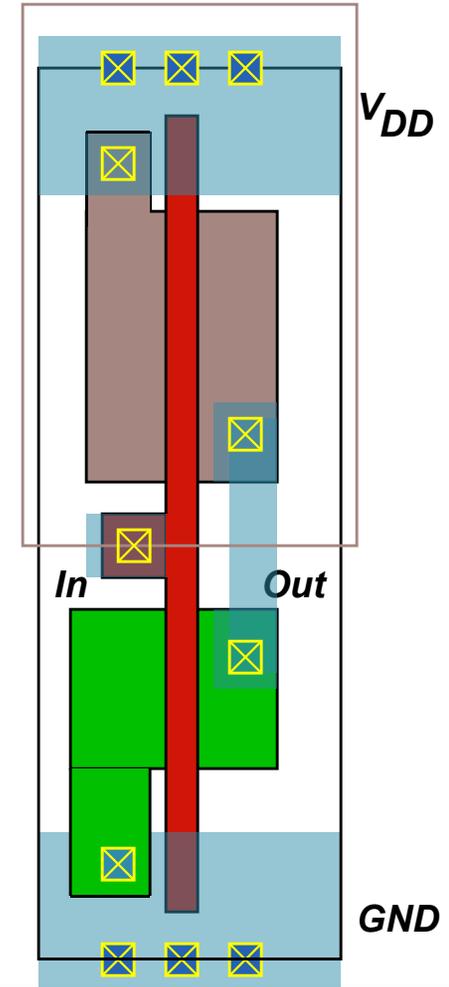
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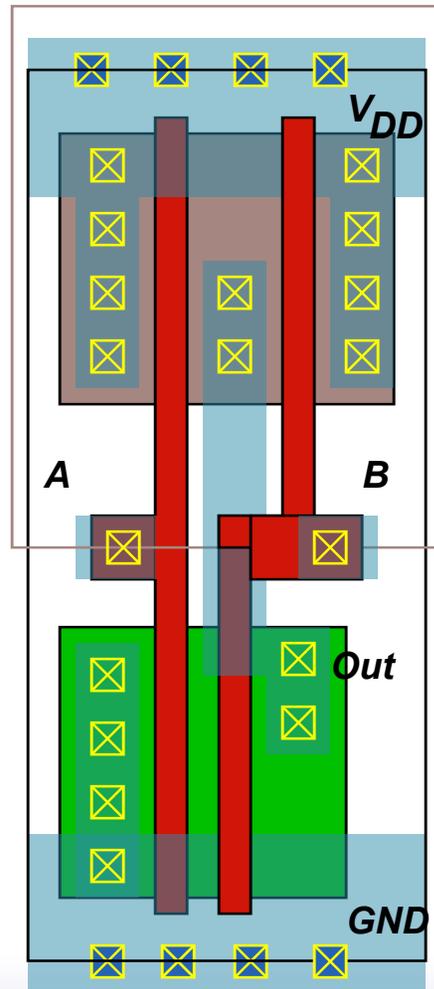
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