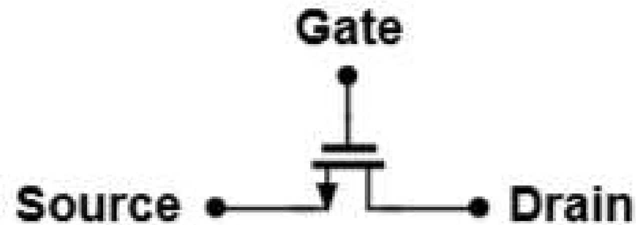
MOSFET as a Switch



- When gate voltage is high, device is on.
- Source and drain are interchangeable.
- But,
  - At what gate voltage does the device turn on?
  - How much is the resistance between S and D?
  - What limits the speed of the device?

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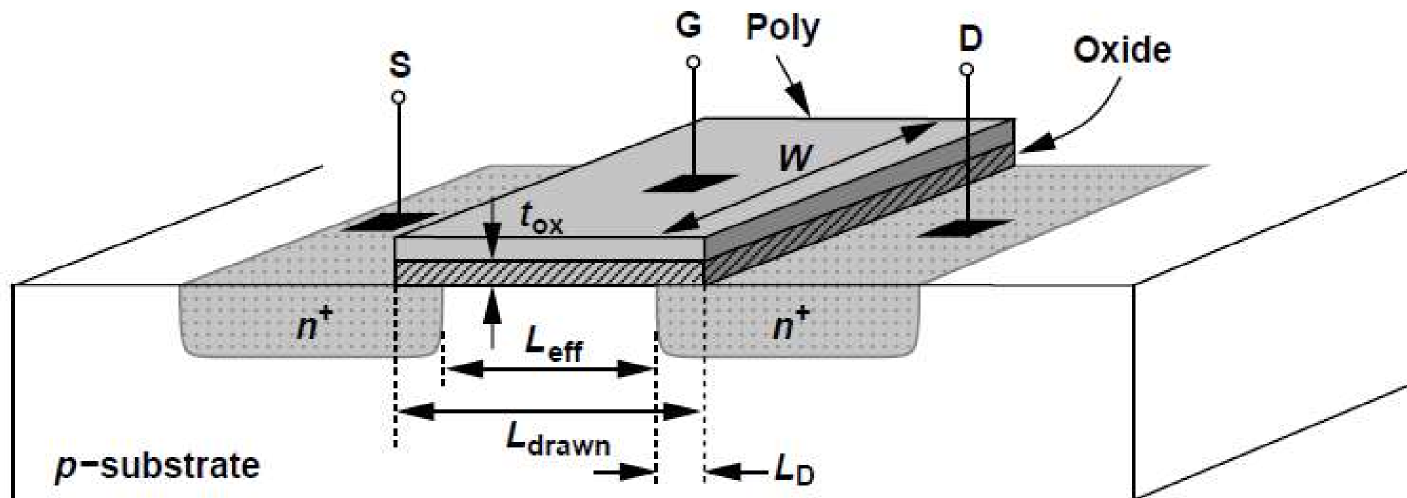
MOSFET Structure



- *n*-type MOS (NMOS) has *n*-doped source (S) and drain (D) on *p*-type substrate (“bulk” or “body”).
- S/D junctions “side-diffuse” during fabrication so that effective length $L_{eff} = L_{drawn} - 2L_D$.
- Typical values are $L_{eff} \approx$ 10 nm and $t_{ox} \approx$ 15 Å.
- The S terminal provides charge carriers and the D terminal collects them.
- As voltages at the three terminals changes, the source and drain may exchange roles.

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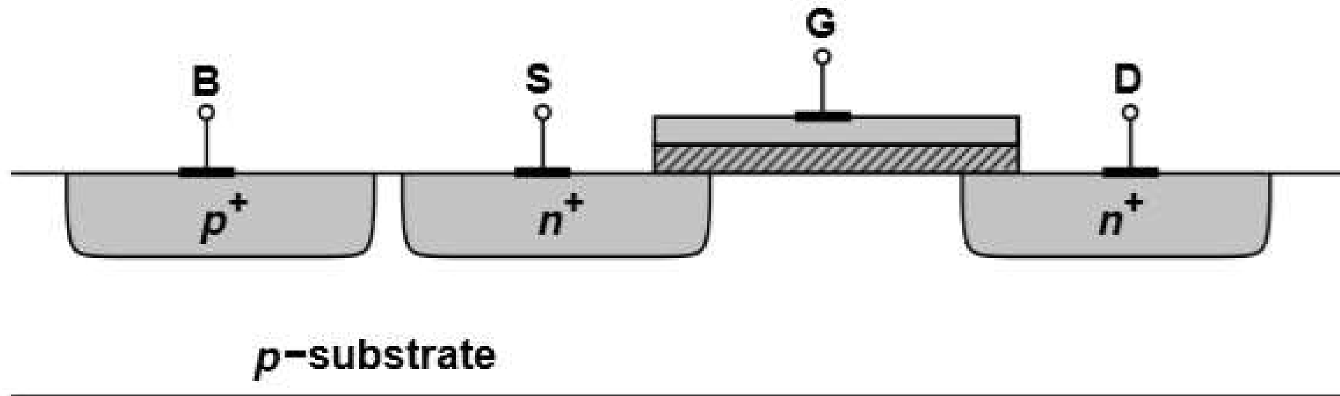
MOSFET Structure



- **MOSFETs actually have *four* terminals.**
- **Substrate potential greatly influences device characteristics.**
- **Typically S/D junction diodes are reversed-biased and the NMOS substrate is connected to the most negative supply in the system.**

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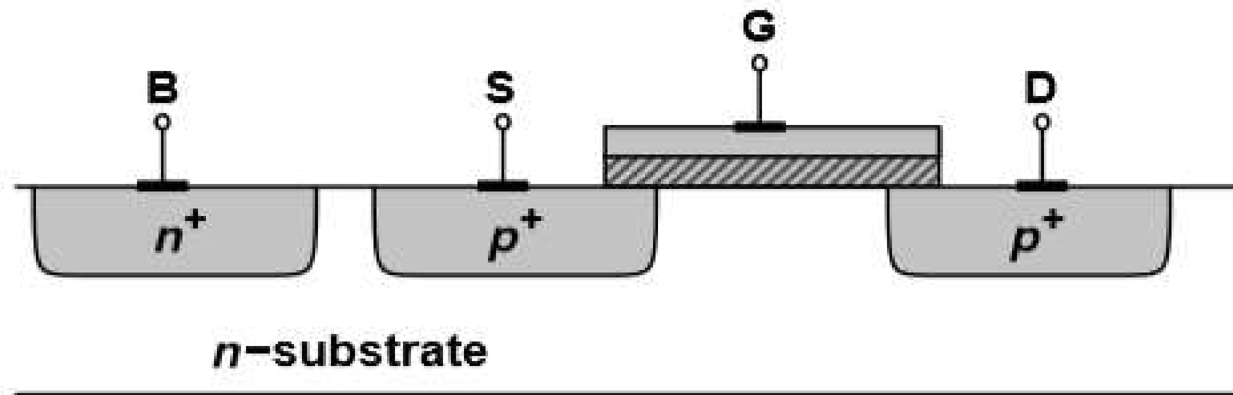
MOSFET Structure



- **PMOS is obtained by inverting all of the doping types (including the substrate).**

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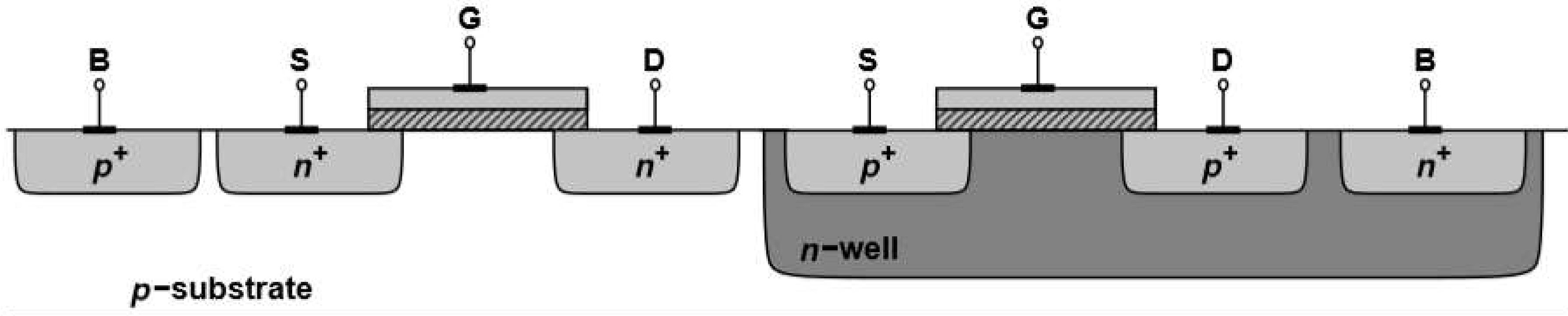
MOSFET Structure



- **In complementary MOS (CMOS) technologies both NMOS (NFET) and PMOS (PFET) are needed and fabricated on the same wafer.**
- **In today's CMOS, the PMOS is fabricated in an *n*-well, where the *n*-well is tied to the most positive supply voltage.**

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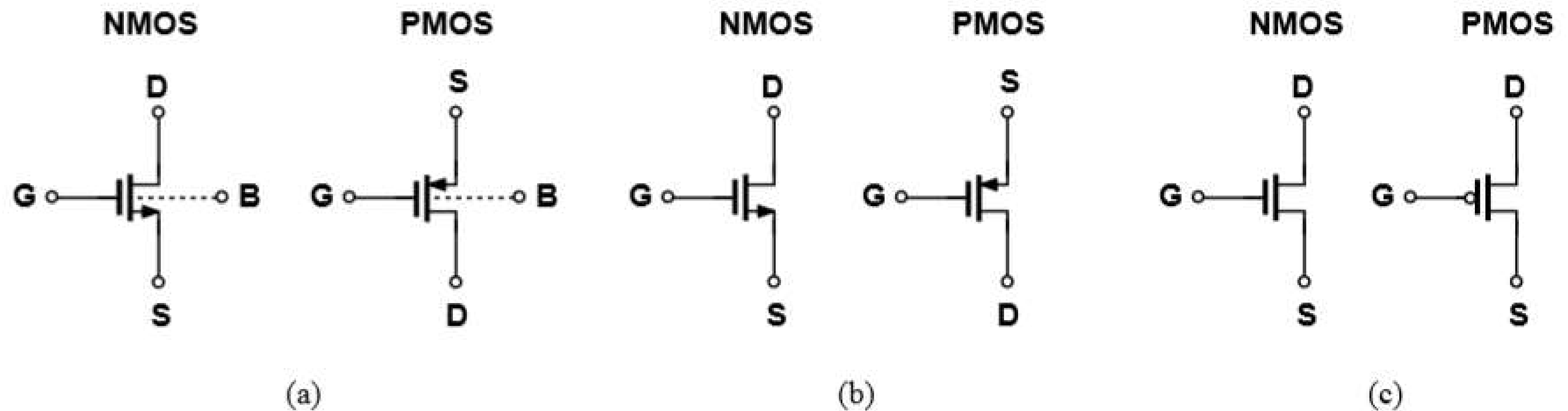
MOS Symbols



- **Substrate is denoted by “B” (bulk).**
- **PMOS source is positioned on top since it has a higher potential than the gate.**
- **Most circuits have NMOS and PMOS bulk tied to ground and V_{DD}, respectively, so we tend to omit the connections (b,c).**
- **Digital circuits tend to incorporate “switch” symbols (c).**

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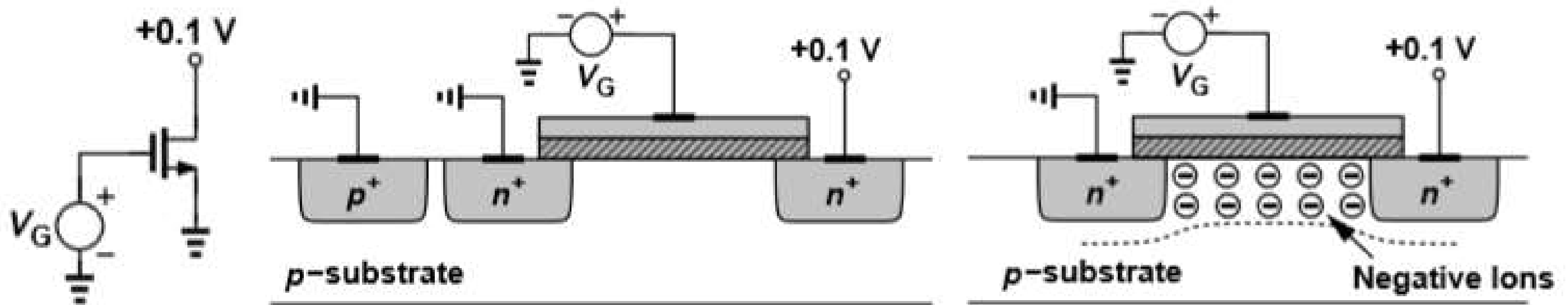
Threshold Voltage



- As V_G increases from zero, holes in *p*-substrate are repelled leaving negative ions behind to form a depletion region.
- There are no charge carriers, so no current flow.

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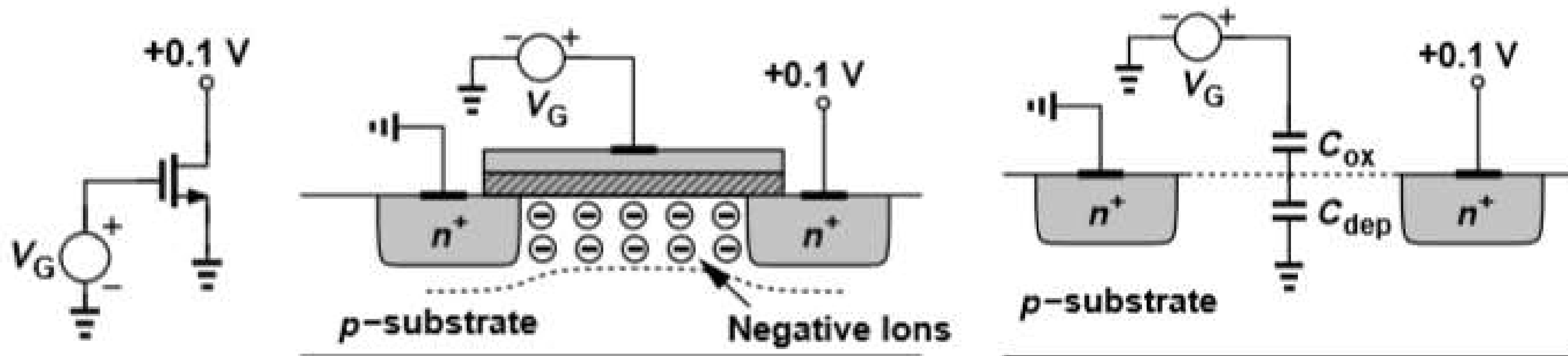
Threshold Voltage



- Increasing V_G further increases the width of the depletion region and the potential at the oxide-silicon interface.
- Structure resembles voltage divider consisting of gate-oxide capacitor and depletion region capacitor in series.

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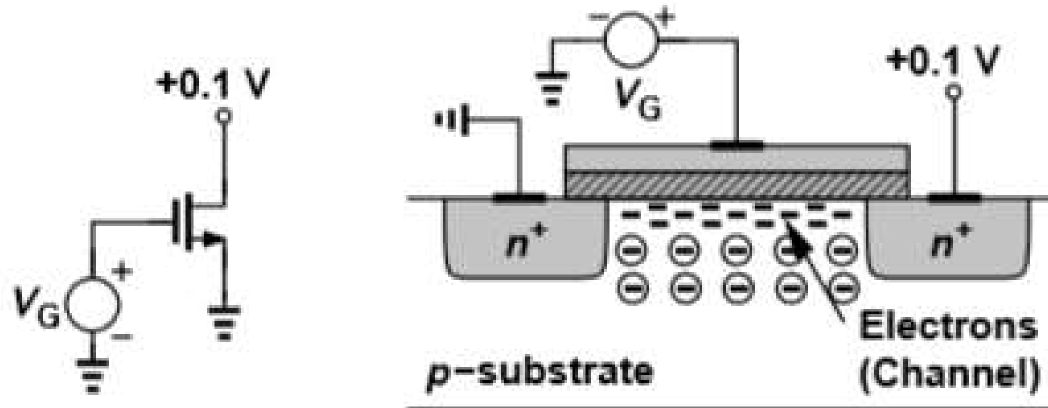
Threshold Voltage



- When interface potential reaches sufficiently positive value, electrons flow from the source to the interface and eventually to the drain.
- This creates a channel of charge carriers (inversion layer) beneath the gate oxide.
- The value of V_G at which the inversion layer occurs is the threshold voltage (V_{TH}).

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Threshold Voltage

$$V_{TH} = \Phi_{MS} + 2\Phi_F + \frac{Q_{dep}}{C_{ox}}.$$

$$\Phi_F = (kT/q)\ln(N_{sub}/n_i). \qquad Q_{dep} = \sqrt{4q\epsilon_{si}|\Phi_F|N_{sub}}.$$

- **Where**

  - Φ_{MS} is the difference between the work functions of the polysilicon gate and the silicon substrate.

  - k is Boltzmann's constant.

  - q is the electron charge.

  - N_{sub} is the doping density of the substrate.

  - n_i is the density of electrons in undoped silicon.

  - Q_{dep} is the charge in the depletion region.

  - C_{ox} is the gate oxide capacitance per unit area.

  - ϵ_{si} is the dielectric constant of silicon.

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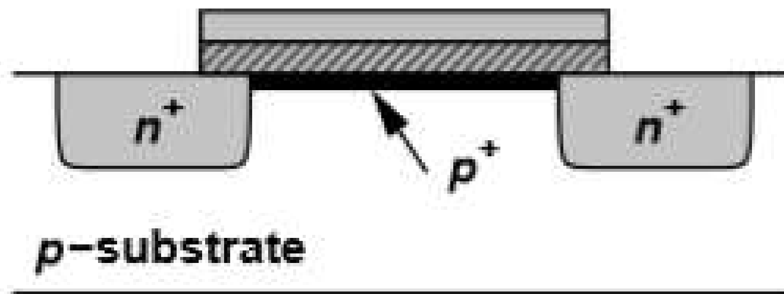
Threshold Voltage



- In practice, threshold voltage is adjusted by implanting dopants into the channel area during device fabrication.
- For NMOS, adding a thin sheet of p^+ increases the gate voltage necessary to deplete the region.

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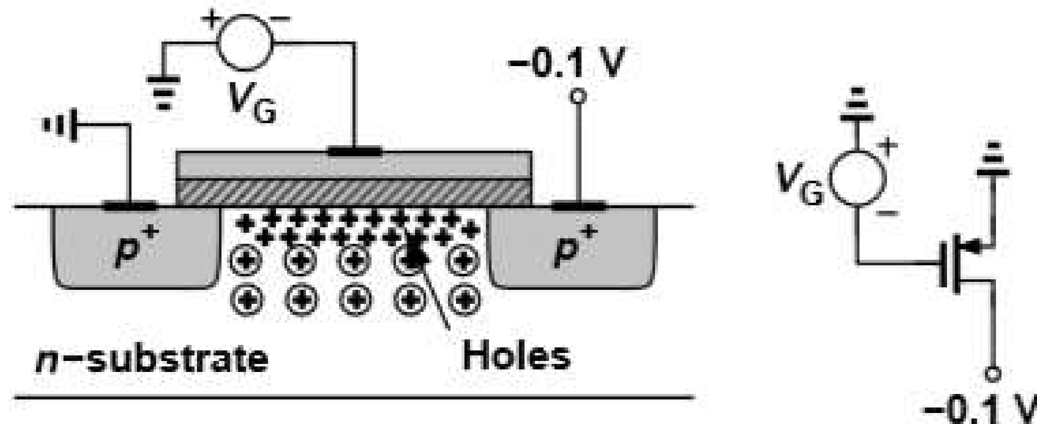
Threshold Voltage



- **Turn-on phenomena in PMOS is similar to that of NMOS but with all polarities reversed.**
- **If the gate-source voltage becomes sufficiently *negative*, an inversion layer consisting of holes is formed at the oxide-silicon interface, providing a conduction path between source and drain.**
- **PMOS threshold voltage is negative.**

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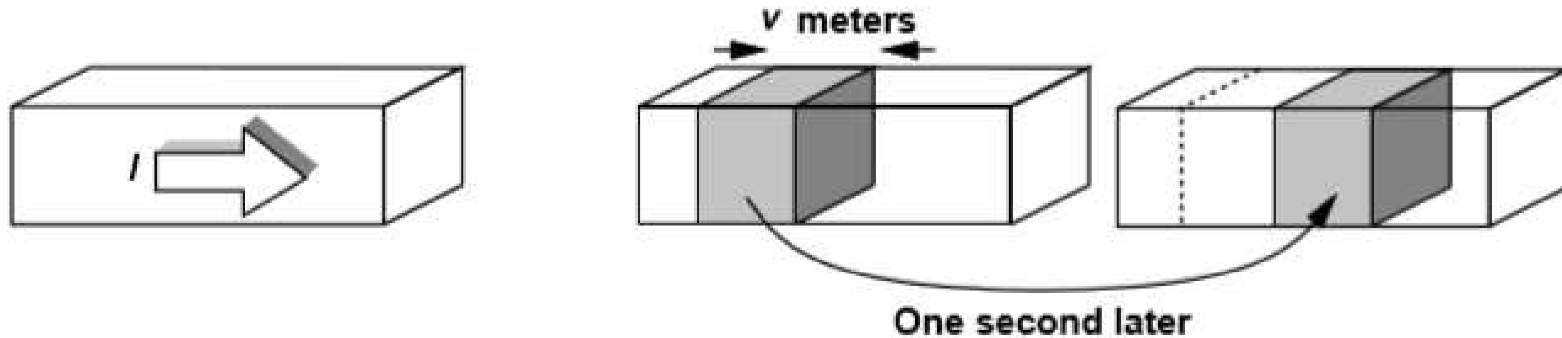
Derivation of I/V Characteristics



$$I = Q_d \cdot v$$

- **Where**

  - Q_d is the mobile charge density along the direction of current I.

  - v is the charge velocity.

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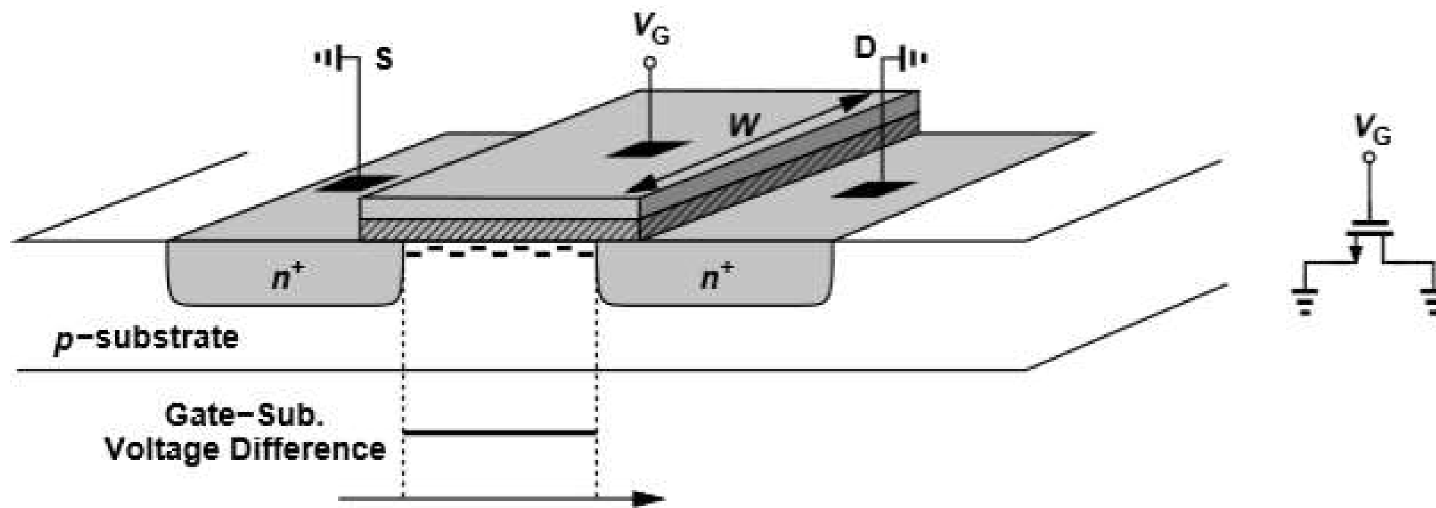
Derivation of I/V Characteristics



- **Onset of inversion occurs at $V_{GS} = V_{TH}$.**
- **Inversion charge density produced by gate oxide capacitance is proportional to $V_{GS} - V_{TH}$ since for $V_{GS} \geq V_{TH}$, charge placed on the gate must be mirrored by charge in the channel, yielding a uniform channel charge density:**

$$Q_d = WC_{ox}(V_{GS} - V_{TH}).$$

- **Where WC_{ox} is the total capacitance per unit length.**

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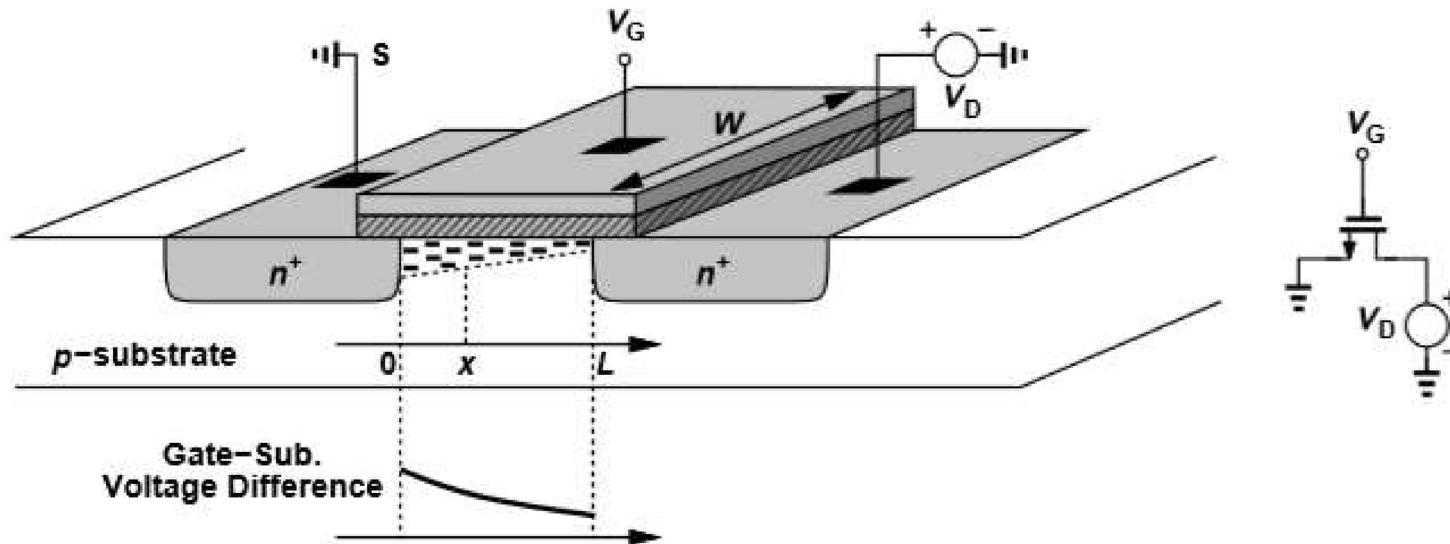
Derivation of I/V Characteristics



- **Channel potential varies from zero at the source to V_D at the drain.**
- **Local voltage *difference* between the gate and the channel varies from V_G to $V_G - V_D$.**
- **Charge density now varies with respect to x :**

$$Q_d(x) = WC_{ox}[V_{GS} - V(x) - V_{TH}],$$

where V(x) is the channel potential at x.

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Derivation of I/V Characteristics

$$I_D = \mu_n C_{ox}\left(\frac{W}{L}\right)\left[(V_{GS} - V_{TH})V_{DS} - \left(\frac{1}{2}\right)V_{DS}^2\right].$$

- **Since**
  - $I = Q_d \cdot v.$
  - $v = \mu E.$
  - $E(x) = -dV/dx.$
  - $Q_d(x) = WC_{ox}[V_{GS} - V(x) - V_{TH}].$
  - $I_D = WC_{ox}[V_{GS} - V(x) - V_{TH}]\mu_n(dV(x)/dx).$
  - $\int_{x=0}^{L} I_D dx = \int_{V=0}^{V_{DS}} WC_{ox}\mu_n[V_{GS} - V(x) - V_{TH}]dV.$

- **A negative sign is added because the charge carriers are negative for NMOS.**

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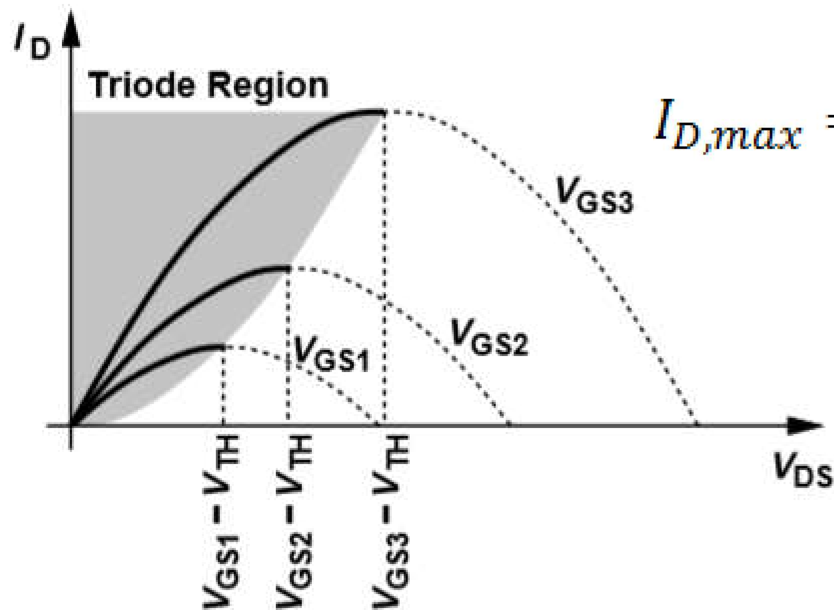
Derivation of I/V Characteristics

$$I_D = \mu_n C_{ox}\left(\frac{W}{L}\right)\left[(V_{GS} - V_{TH})V_{DS} - \left(\frac{1}{2}\right)V_{DS}^2\right].$$



$$I_{D,max} = \left(\frac{1}{2}\right)\mu_n C_{ox}\left(\frac{W}{L}\right)(V_{GS} - V_{TH})^2.$$

- **V_{GS}−V_{TH} is known as the "overdrive voltage."**
- **W/L is known as the "aspect ratio."**
- **If $V_{DS} \le V_{GS}-V_{TH}$, we say the device is operating in the "triode region."**

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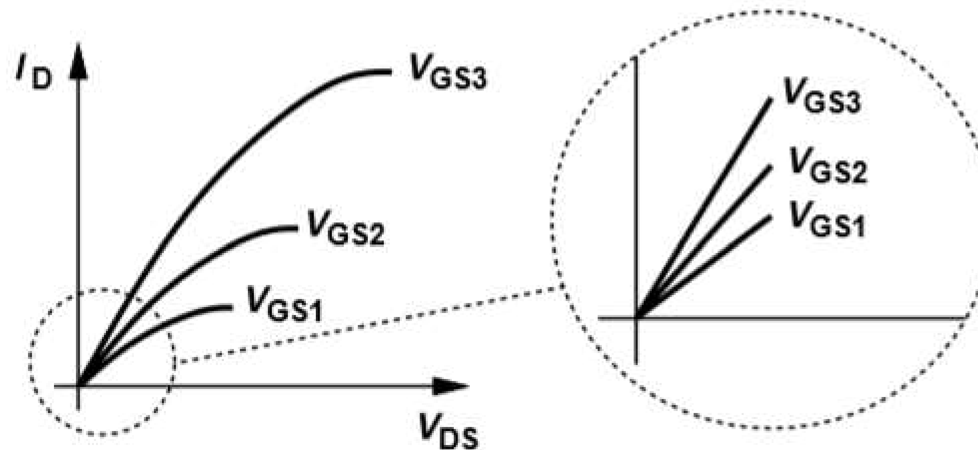
Derivation of I/V Characteristics



- **If $V_{DS} << 2(V_{GS}-V_{TH})$, then**

$$I_D \approx \mu_n C_{ox}\left(\frac{W}{L}\right)(V_{GS}-V_{TH})V_{DS}.$$

- **In this case, the drain current is a linear function of V_{DS} so the path from source to drain can be represented by a linear resistor:**

$$R_{on} = \frac{1}{\mu_n C_{ox}\left(\frac{W}{L}\right)(V_{GS}-V_{TH})}.$$

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Derivation of I/V Characteristics

- If $V_{DS} << 2(V_{GS}-V_{TH})$, the device is operating in “deep triode region.”
- In this region, a MOSFET can operate as a resistor whose value is controlled by the overdrive voltage.
- Unlike bipolar transistors, a MOS device may be on even if it carries no current.

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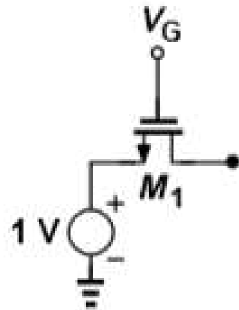
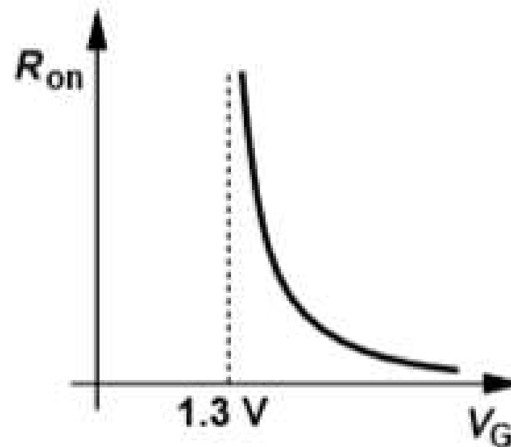
Derivation of I/V Characteristics



- For example, given the topology on the left and that
  - $\mu_n C_{ox} = 50\ \mu\text{A/V}^2$,
  - $W/L = 10$,
  - $V_{TH} = 0.3\ \text{V}$,

$$R_{on} = \frac{1}{50\ \mu\text{A}/\text{V}^2 \times 10(V_G - 1\ \text{V} - 0.3\ \text{V})}.$$



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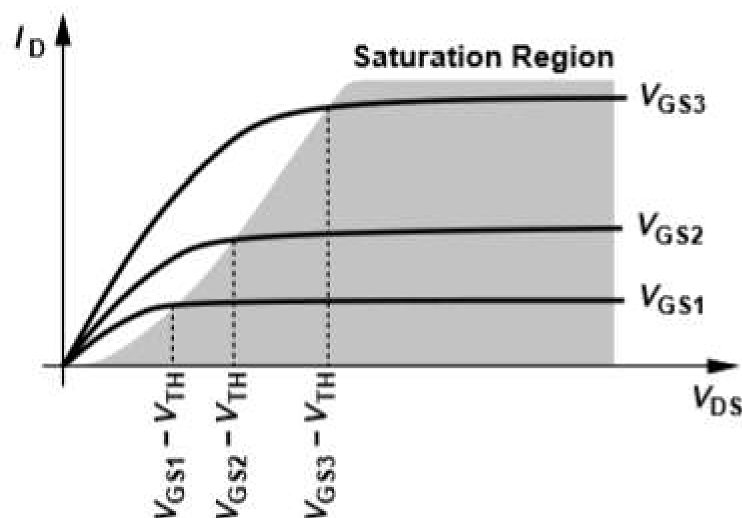
Derivation of I/V Characteristics



- **In reality, if $V_{DS} > V_{GS} - V_{TH}$, I_D becomes relatively constant and we say that the device operates in "saturation region."**
- **$V_{D,sat} = V_{GS} - V_{TH}$ denotes the minimum V_{DS} necessary for operation in saturation.**

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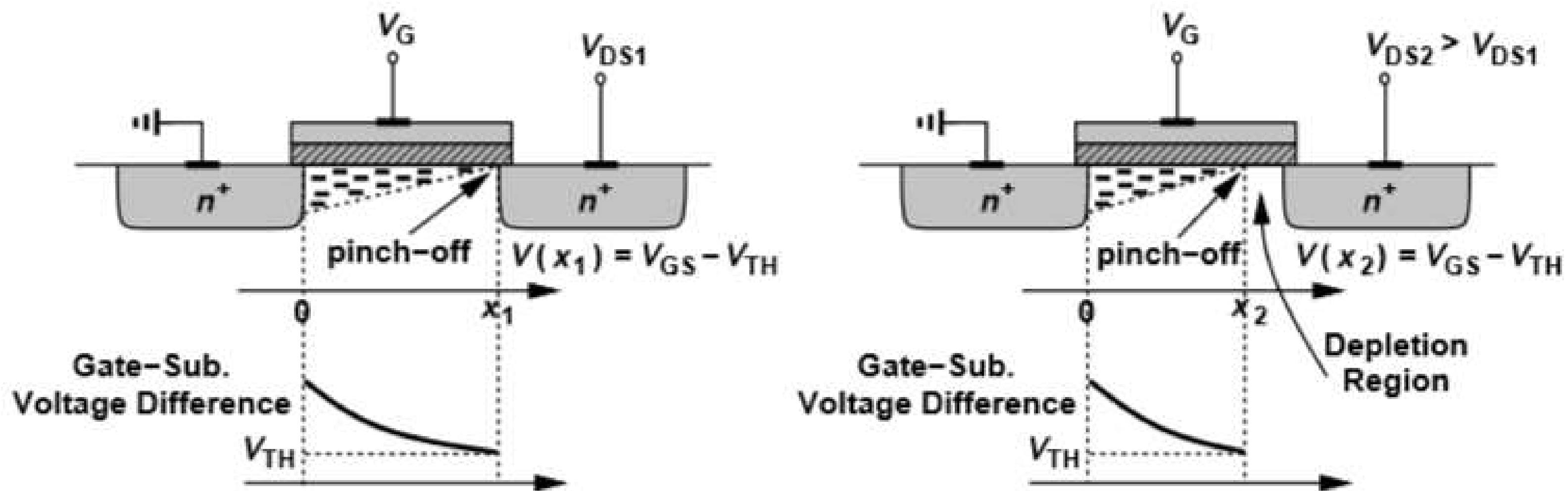
Derivation of I/V Characteristics



- **If V_{DS} is slightly larger than $V_{GS}-V_{TH}$, the inversion layer stops at $x \leq L$, and the channel becomes "pinched off."**
- **As V_{DS} increases, the point at which Q_D equals zero gradually moves towards the source.**
- **At some point along the channel, the local potential difference between the gate and the oxide-silicon interface is not sufficient to support an inversion layer.**

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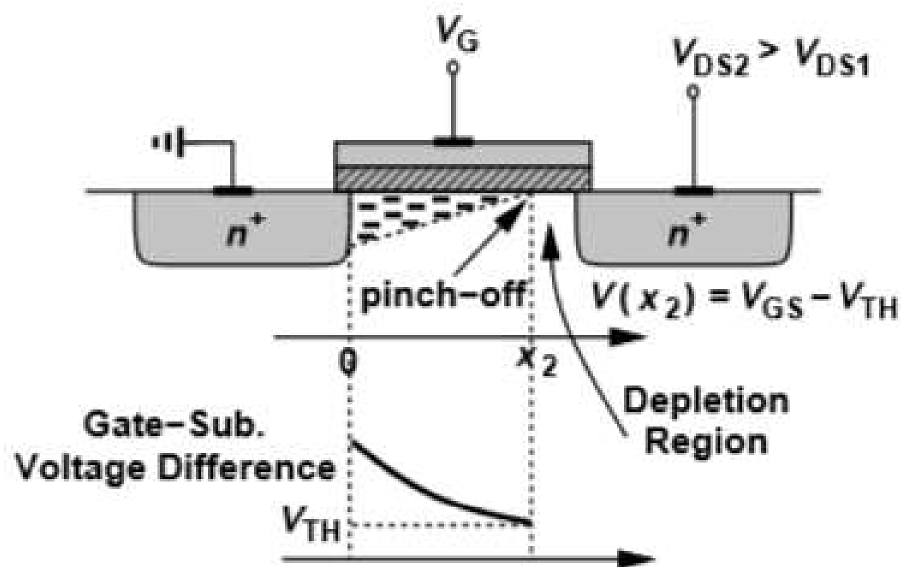
Derivation of I/V Characteristics



- **Electron velocity ($v = I/Q_d$) rises tremendously as they approach the pinch-off point (where $Q_d \to 0$) and shoot through the depletion region near the drain junction and arrive at the drain terminal.**

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Derivation of I/V Characteristics

$$V_{GS} = \sqrt{\frac{2I_D}{\mu_n C_{ox}\frac{W}{L'}}} + V_{TH}$$

- **Since the integral becomes**
  - $\int_{x=0}^{x=x_2=L'} I_D dx = \int_{V=0}^{V=V_{GS}-V_{TH}} W C_{ox}\mu_n [V_{GS} - V(x) - V_{TH}] dV .$

    $I_D = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L'}\right)(V_{GS} - V_{TH})^2.$
  -
- **I_D is relatively independent of V_{DS} if L' remains close to L.**
- **The device exhibits a "square-law" behavior.**

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Derivation of I/V Characteristics

- For PMOS devices, the equations become
  - $I_D = -\mu_p C_{ox} \frac{W}{L}\left[(V_{GS} - V_{TH})V_{DS} - \frac{1}{2}V_{DS}^2\right].$
  - $I_D = -\frac{1}{2}\mu_p C_{ox} \frac{W}{L'}(V_{GS} - V_{TH})^2.$
- The negative sign shows up due to the assumption that drain current flows from drain to source, whereas holes in a PMOS flow in the reverse direction.
- V_{GS}, V_{DS}, V_{TH}, and $V_{GS}-V_{TH}$ are negative for a PMOS transistor that is turned on.
- Since the mobility of holes is about ½ the mobility of electrons, PMOS devices suffer from lower "current drive" capability.

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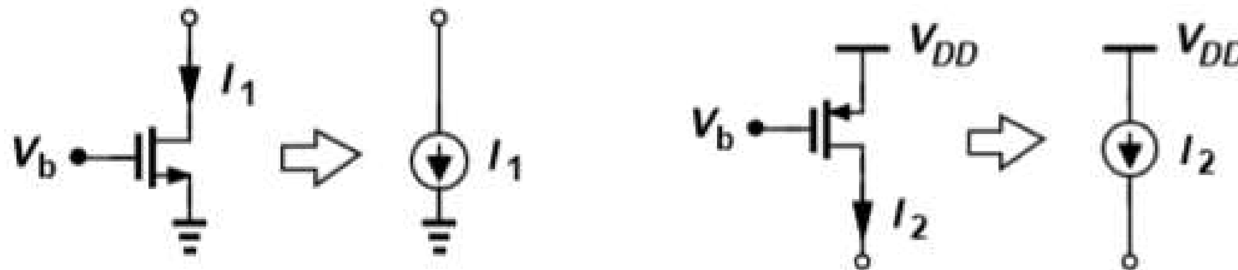
Derivation of I/V Characteristics



- **A saturated MOSFET can be used as a current source connected between the drain and the source.**
- **NMOS current sources inject current into ground while PMOS current sources draws current from V_{DD}.**

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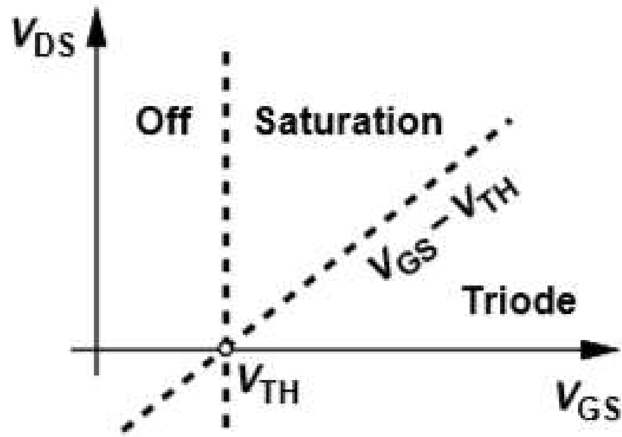
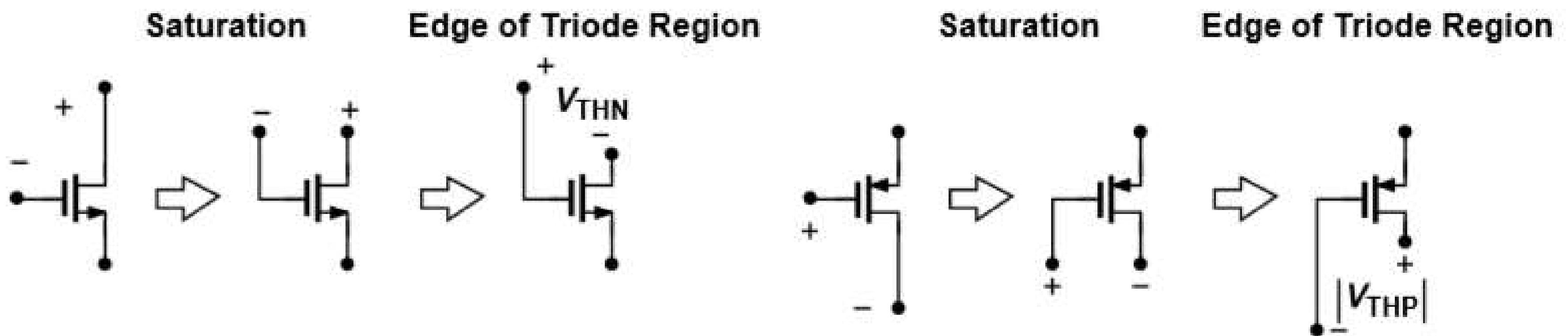
Derivation of I/V Characteristics



- $V_{DS} = V_{GS} - V_{TH} = V_{D,sat}$ **is the line between saturation and triode region.**
- **For a given** V_{DS}**, the device eventually leaves saturation as** V_{GS} **increases.**
- **The drain is defined as the terminal with a higher (lower) voltage than the source for an NMOS (PMOS).**



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