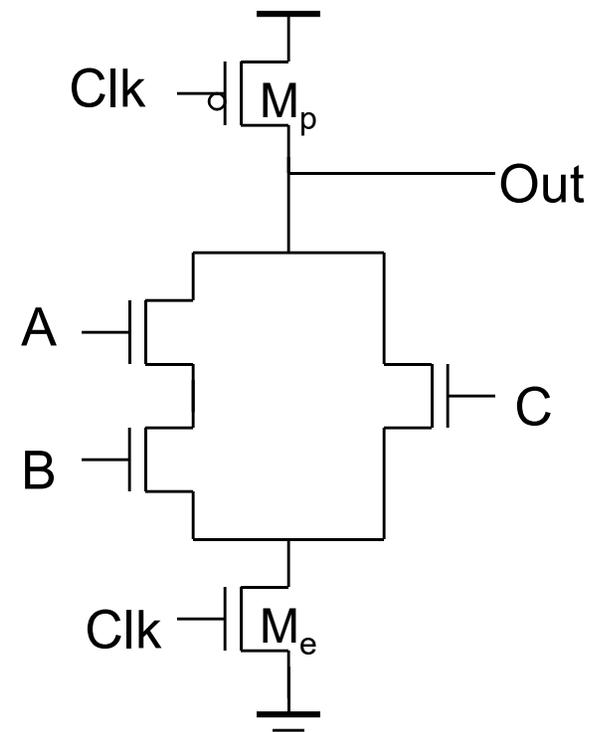
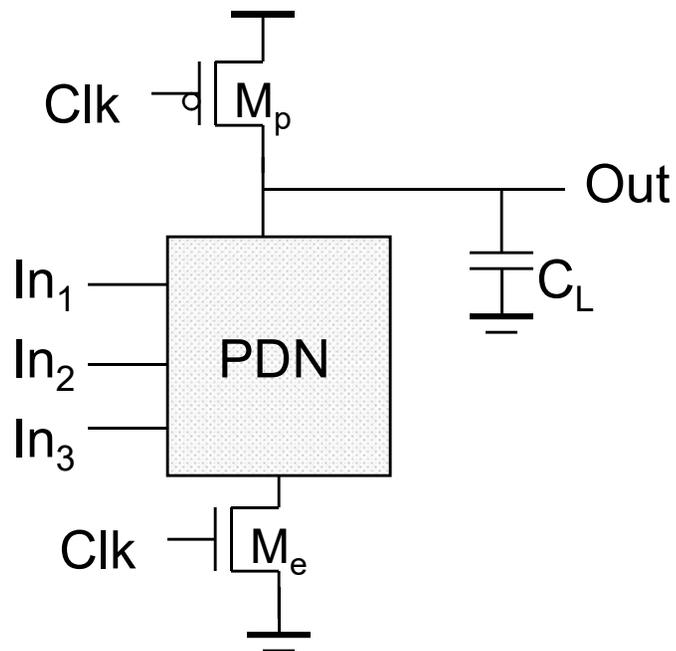


# *Dynamic Logic*

# Dynamic CMOS

- In **static** circuits at every point in time (except when switching) the output is connected to either GND or  $V_{DD}$  via a low resistance path.
  - fan-in of  $n$  requires  $2n$  ( $n$  N-type +  $n$  P-type) devices
- **Dynamic** circuits rely on the temporary storage of signal values on the capacitance of high impedance nodes.
  - requires on  $n + 2$  ( $n+1$  N-type + 1 P-type) transistors

# Dynamic Gate

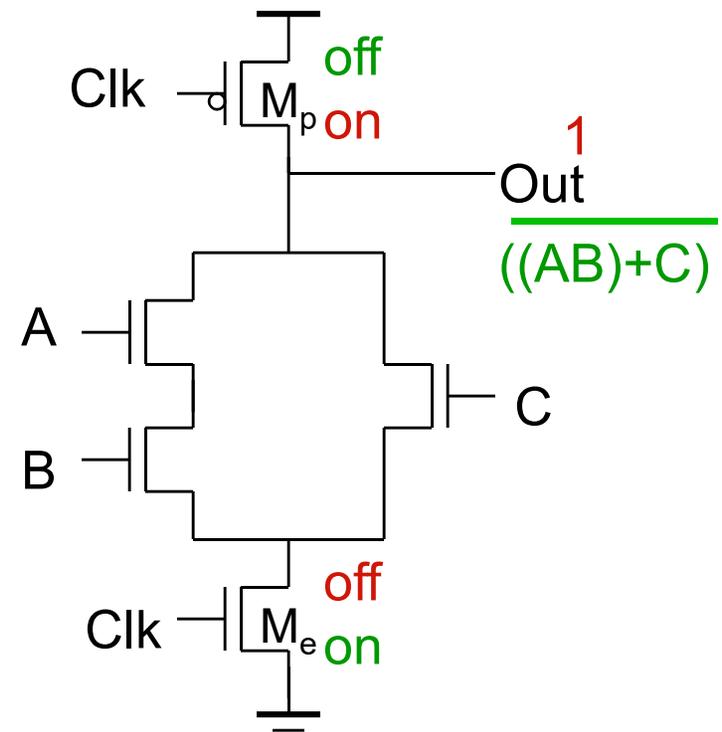
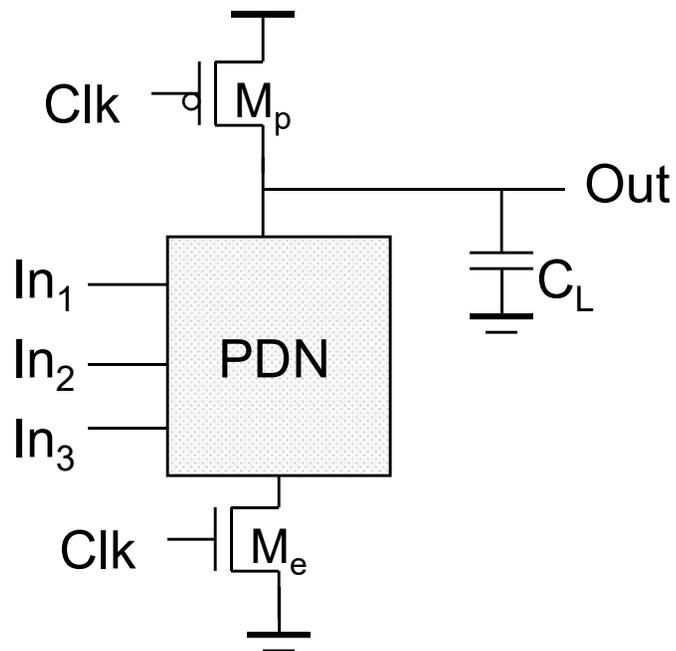


Two phase operation

Precharge (CLK = 0)

Evaluate (CLK = 1)

# Dynamic Gate



Two phase operation

Precharge (Clk = 0)

Evaluate (Clk = 1)

# Conditions on Output

- ❑ Once the output of a dynamic gate is discharged, it cannot be charged again until the next precharge operation.
- ❑ Inputs to the gate can make **at most** one transition during evaluation.
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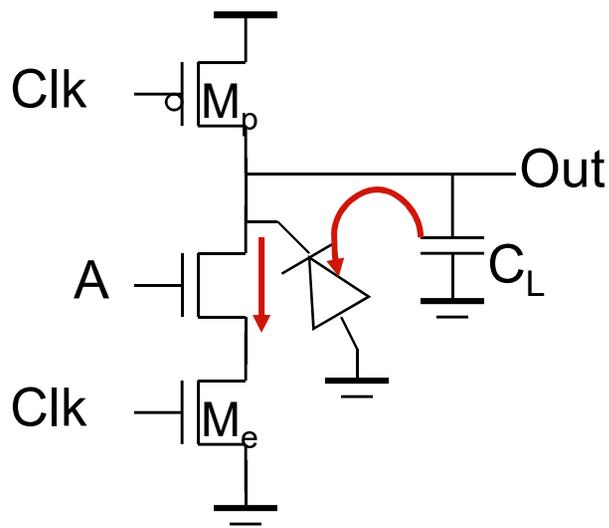
# Properties of Dynamic Gates

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- ❑ Full swing outputs ( $V_{OL} = \text{GND}$  and  $V_{OH} = V_{DD}$ )
- ❑ Non-ratioed - sizing of the devices does not affect the logic levels
- ❑ Faster switching speeds
  - reduced load capacitance due to **lower input** capacitance ( $C_{in}$ )
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  - no  $I_{sc}$ , so all the current provided by PDN goes into discharging  $C_L$

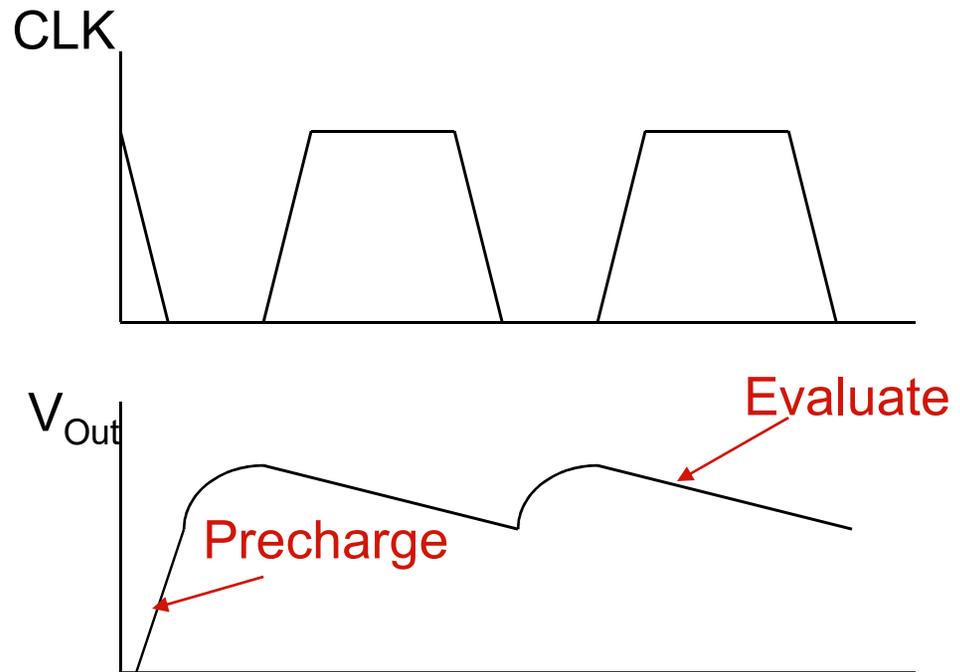
# Properties of Dynamic Gates

- ❑ Overall power dissipation usually **higher** than static CMOS
  - no static current path ever exists between  $V_{DD}$  and GND (including  $P_{sc}$ )
  - no glitching
  - **higher transition probabilities**
  - **extra load on Clk**
- ❑ PDN starts to work as soon as the input signals exceed  $V_{Tn}$ , so  $V_M$ ,  $V_{IH}$  and  $V_{IL}$  equal to  $V_{Tn}$ 
  - low noise margin ( $NM_L$ )
- ❑ Needs a precharge/evaluate clock

# Issues in Dynamic Design 1: Charge Leakage

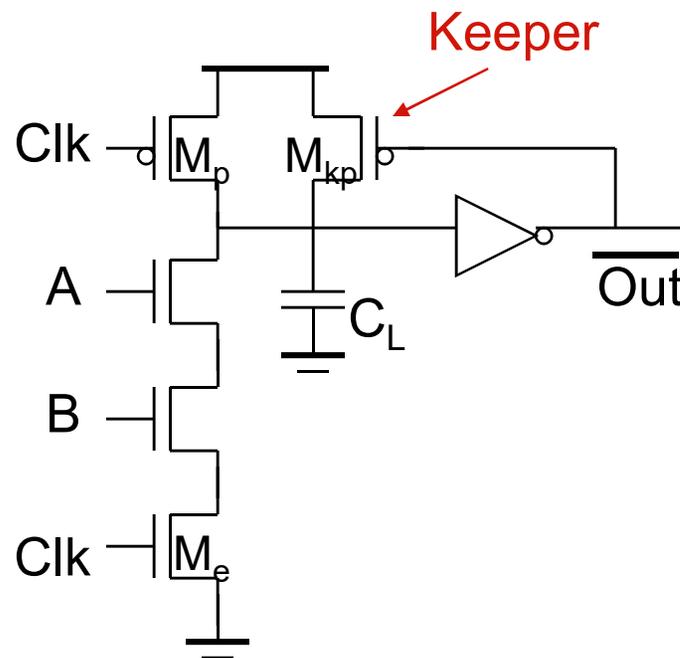


Leakage sources



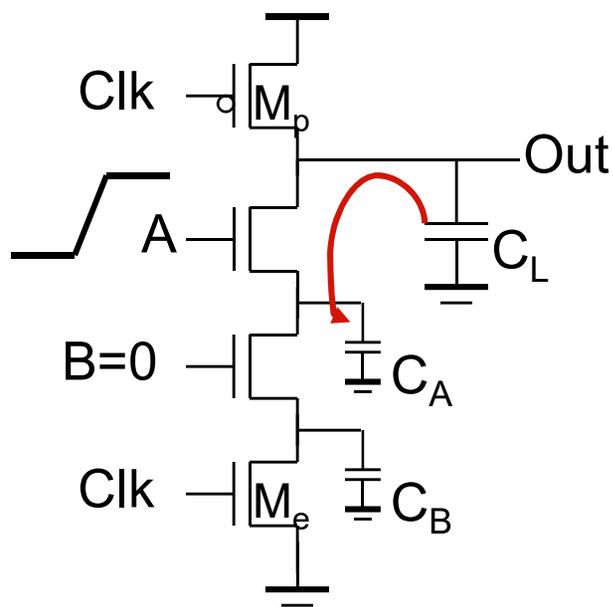
*Dominant component is subthreshold current*

# Solution to Charge Leakage



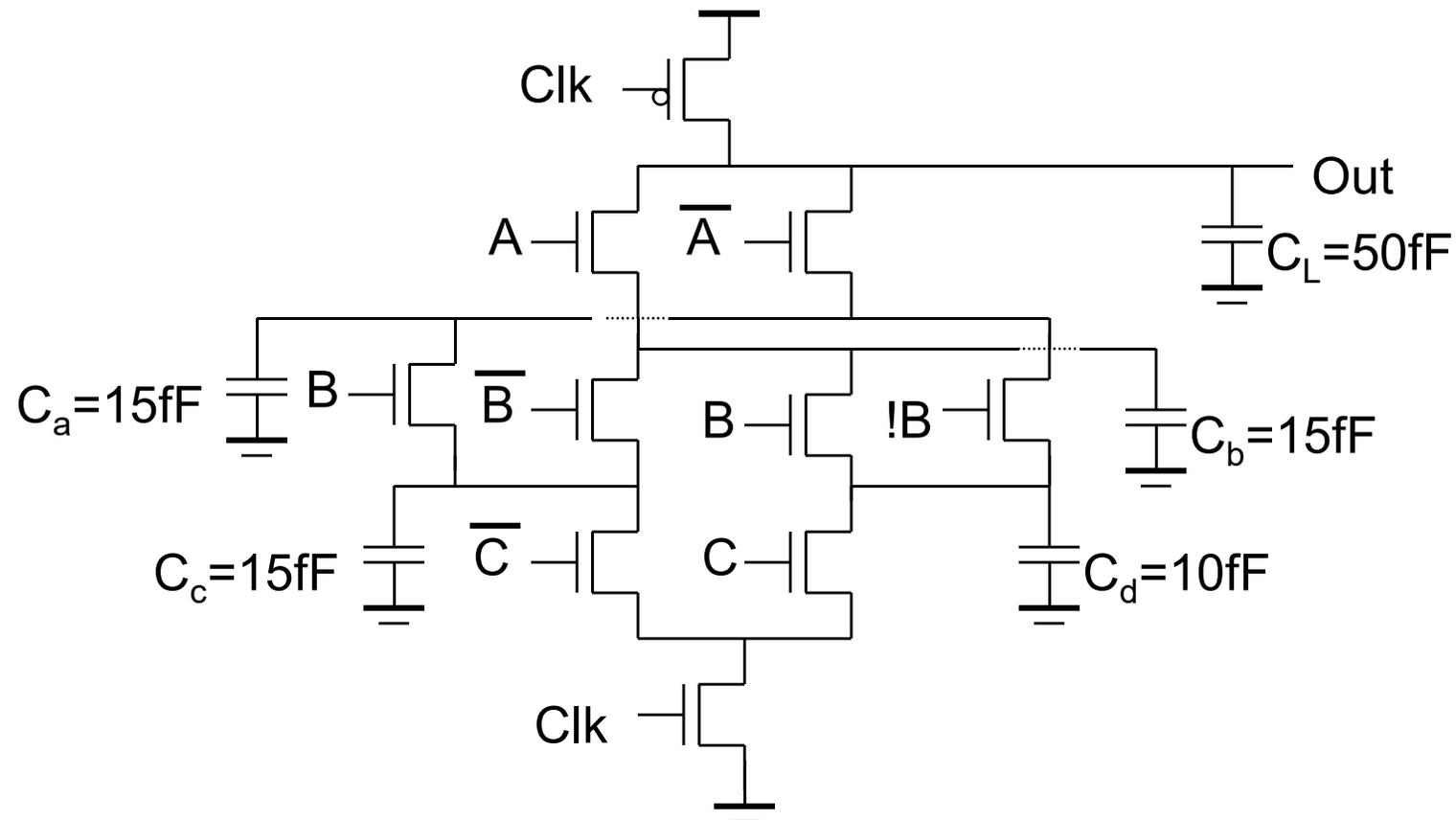
Same approach as level restorer for pass-transistor logic

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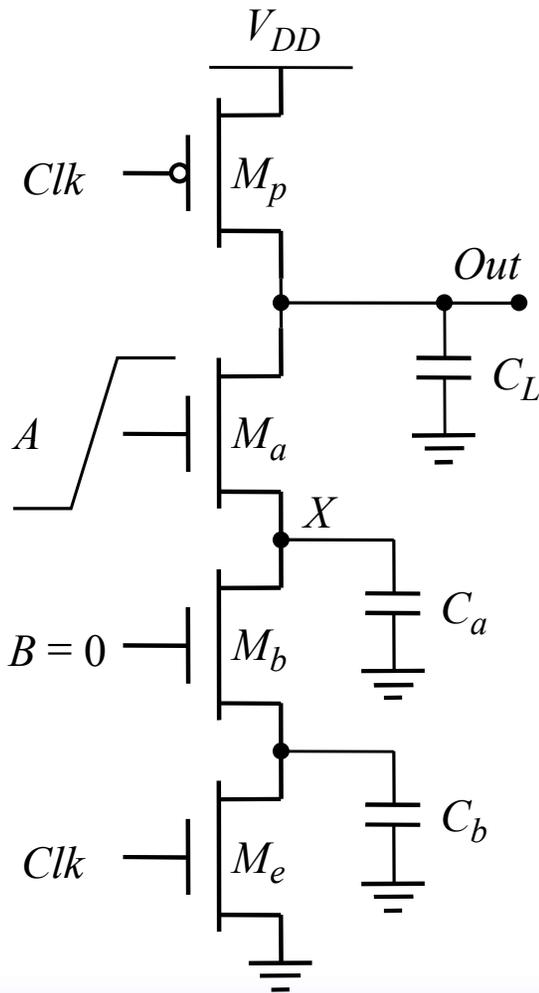


Charge stored originally on  $C_L$  is redistributed (shared) over  $C_L$  and  $C_A$  leading to reduced robustness

# Charge Sharing Example



# Charge Sharing



**case 1) if  $\Delta V_{out} < V_{Tn}$**

$$C_L V_{DD} = C_L V_{out}(t) + C_a (V_{DD} - V_{Tn}(V_X))$$

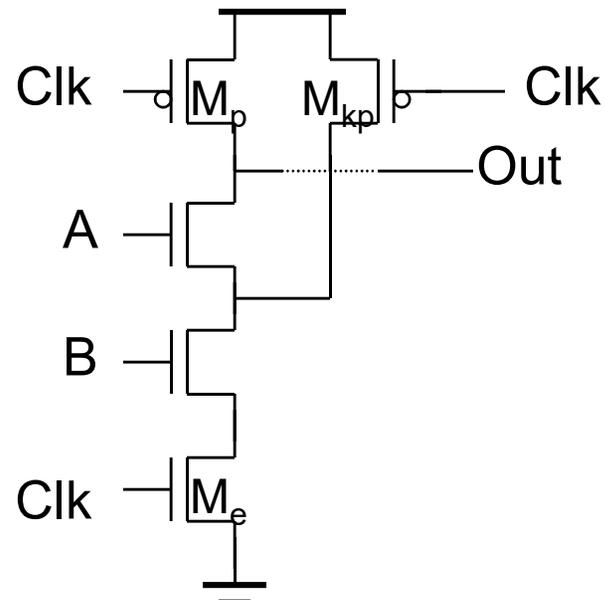
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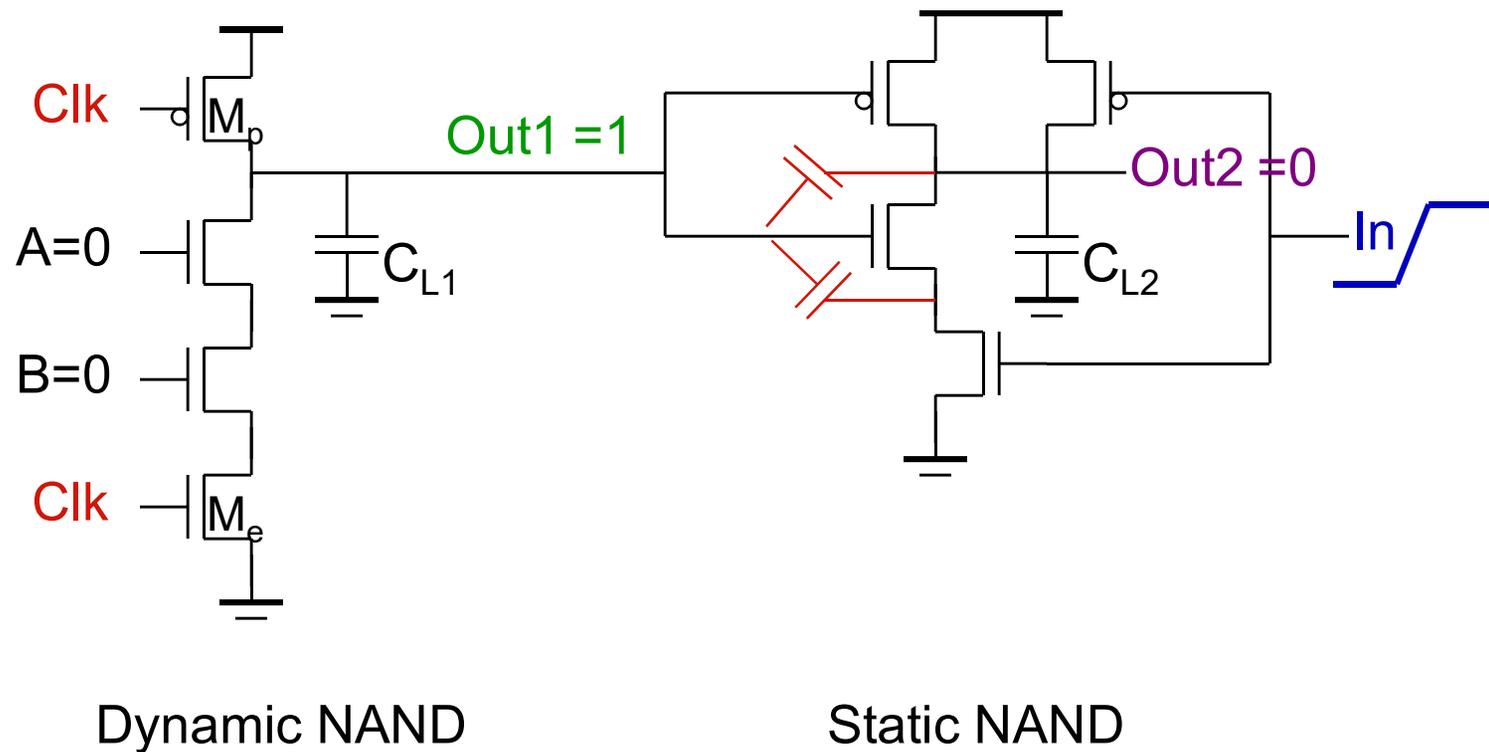
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# *Solution to Charge Redistribution*

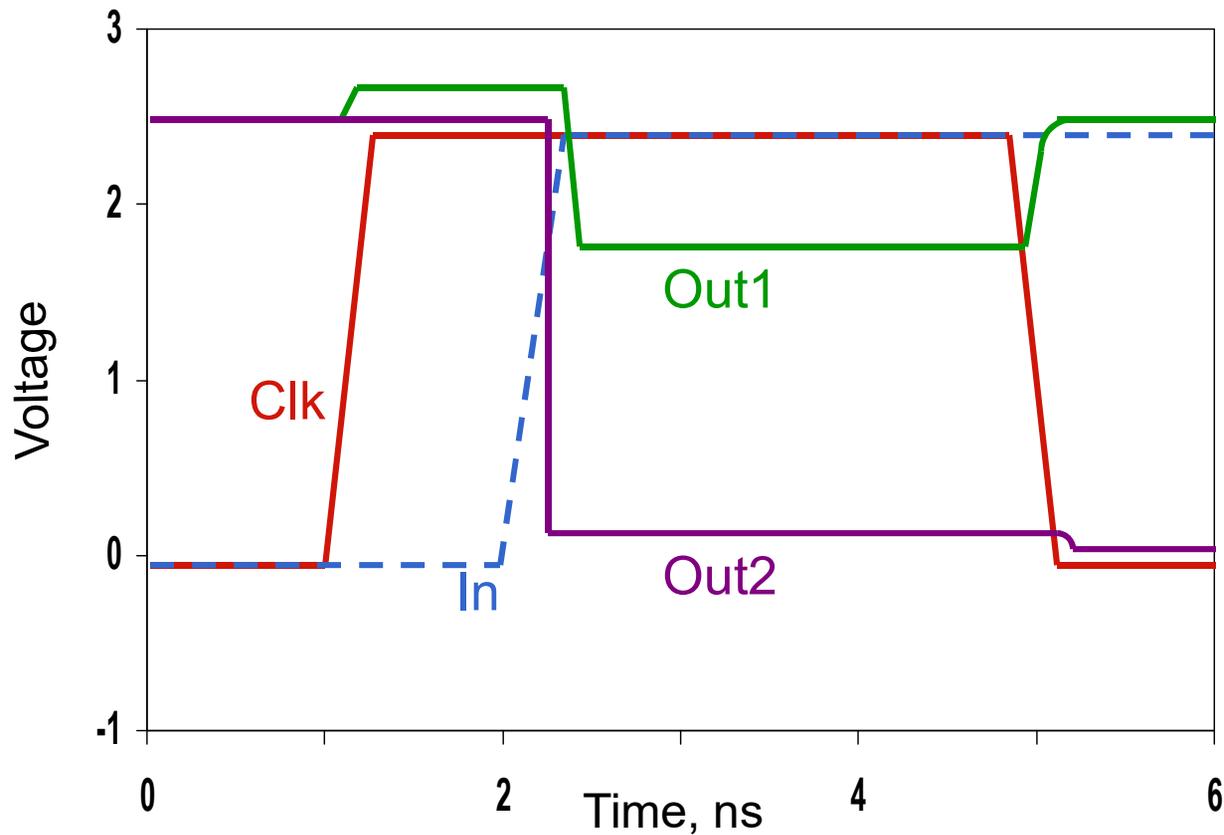


Precharge internal nodes using a clock-driven transistor  
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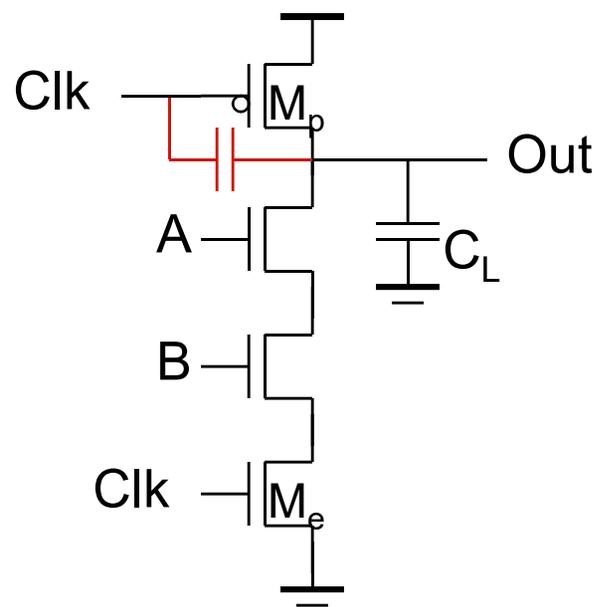
# Issues in Dynamic Design 3: Backgate Coupling



# Backgate Coupling Effect

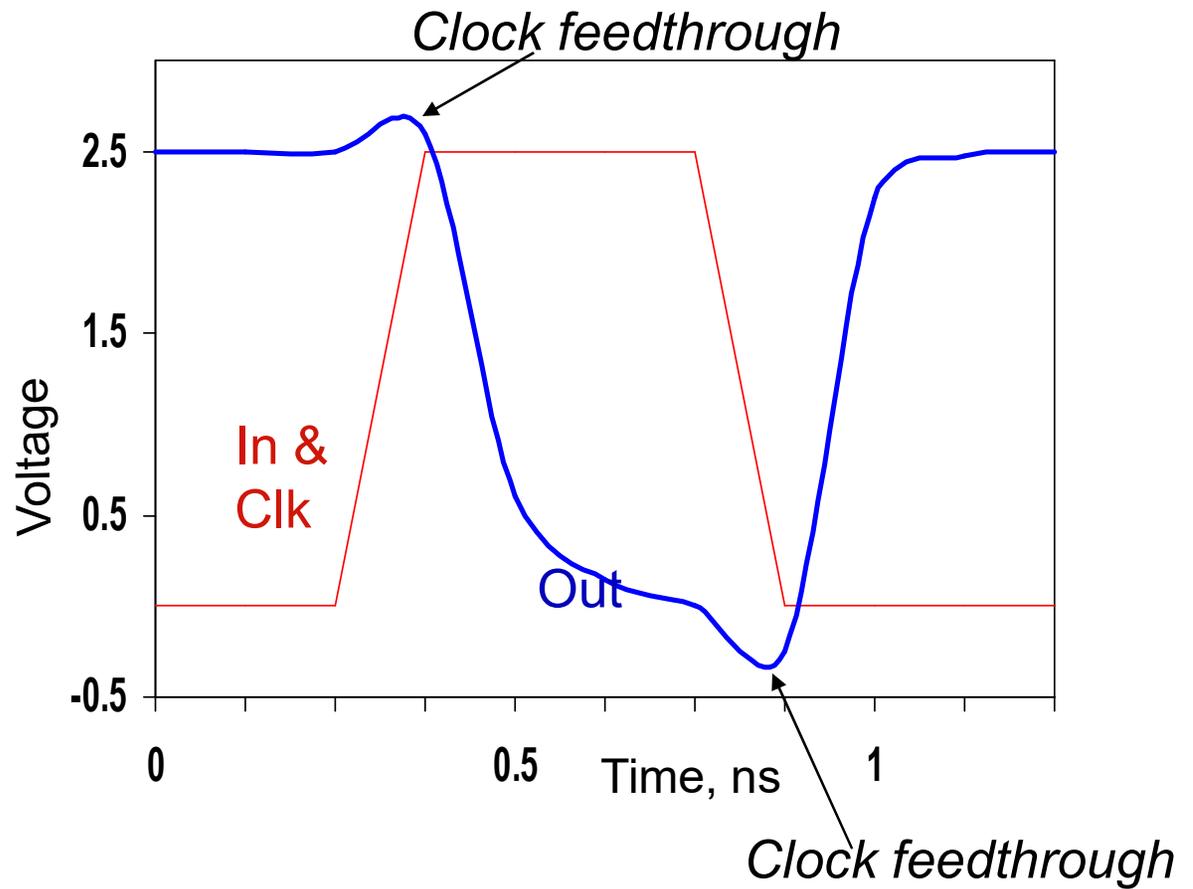
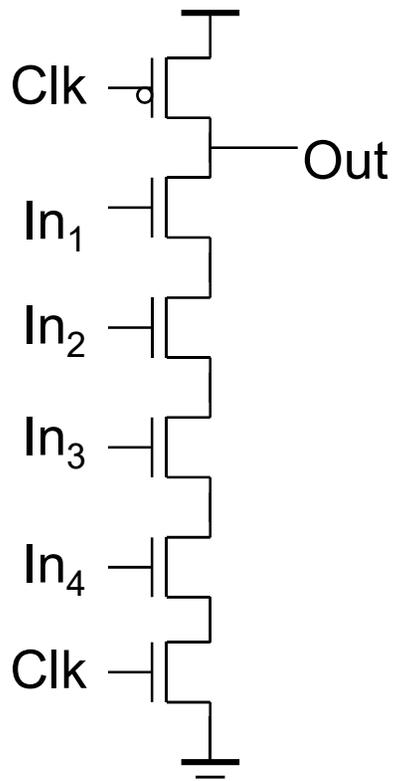


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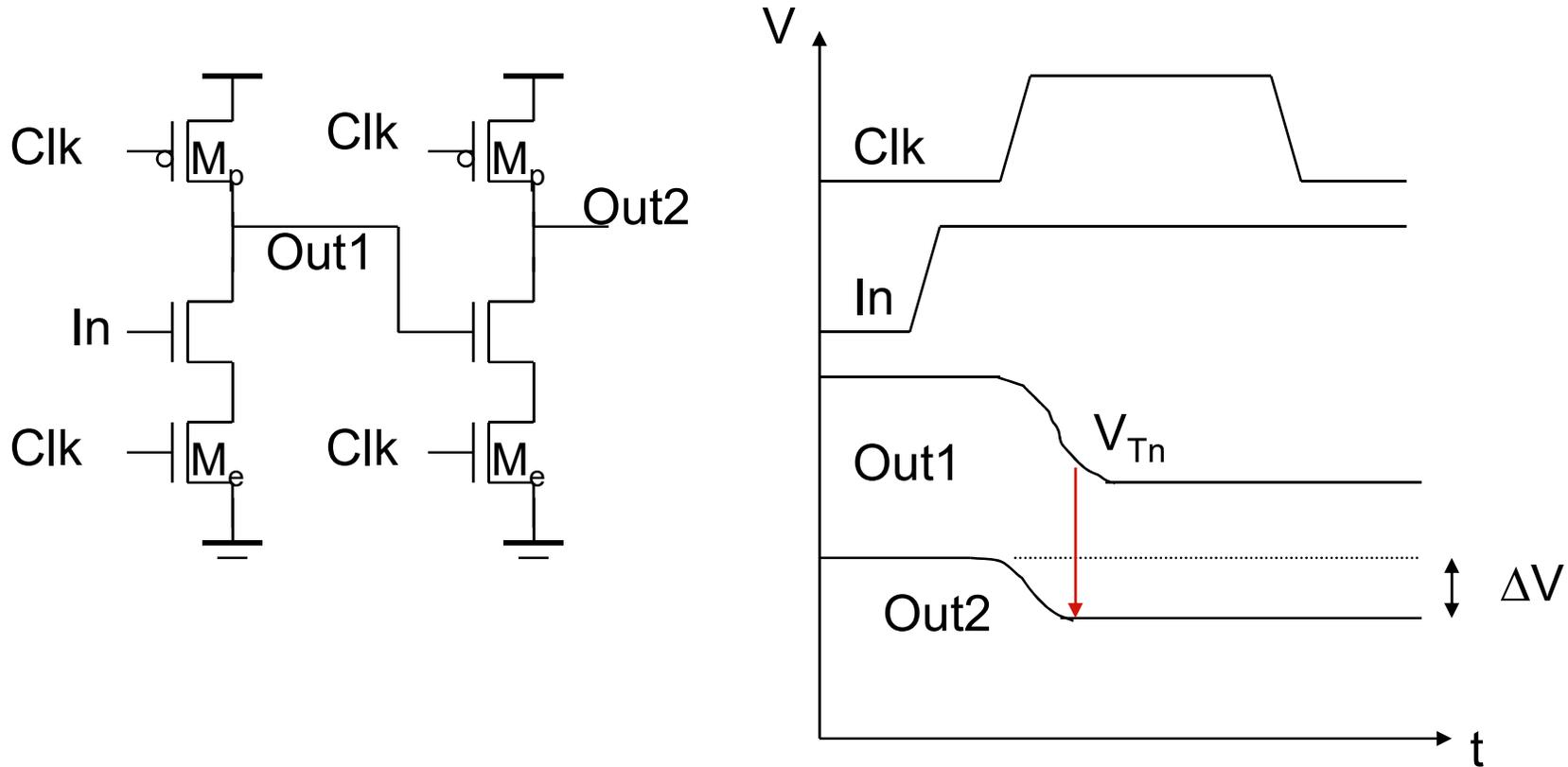
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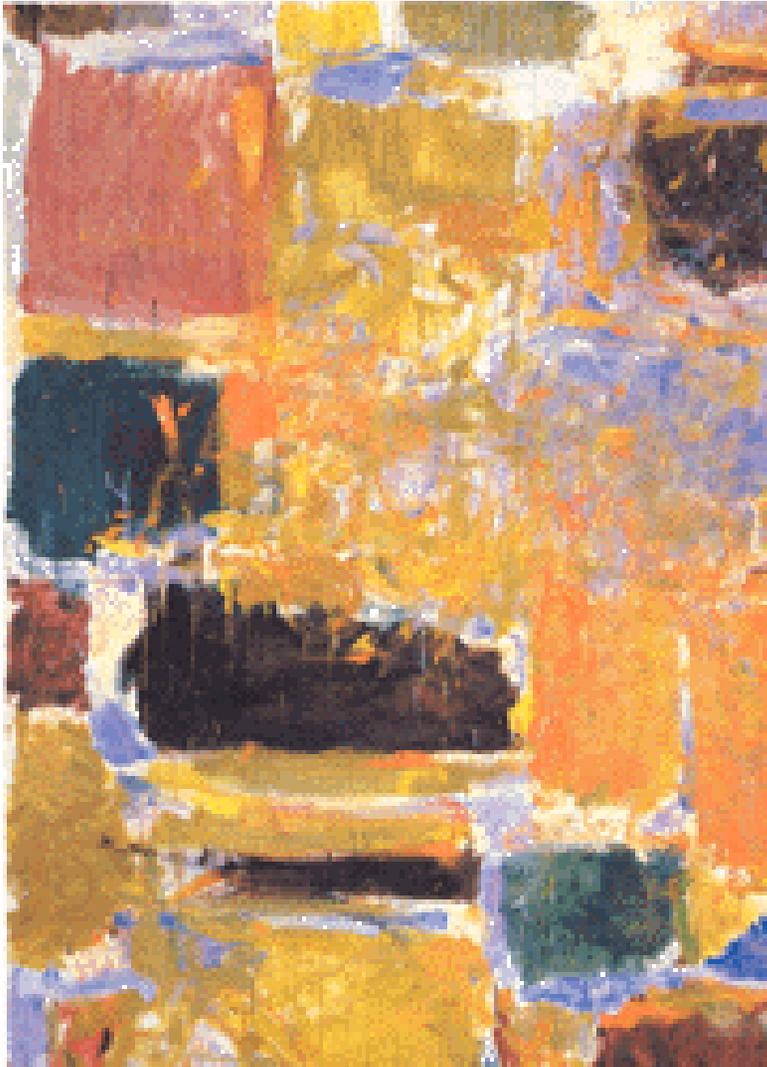
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# Cascading Dynamic Gates



Only 0  $\rightarrow$  1 transitions allowed at inputs!

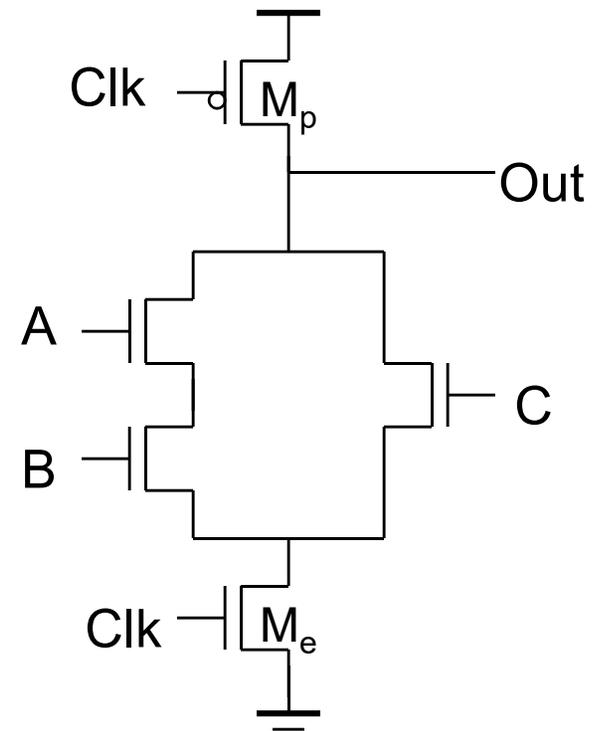
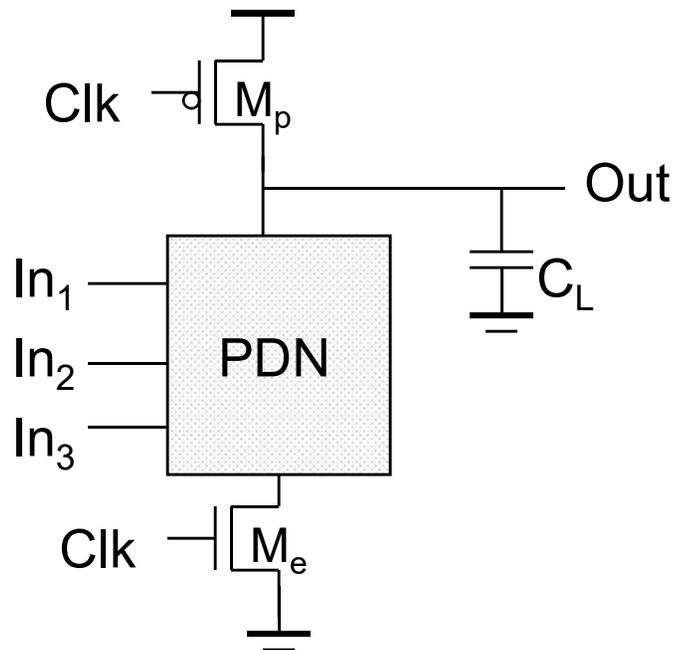


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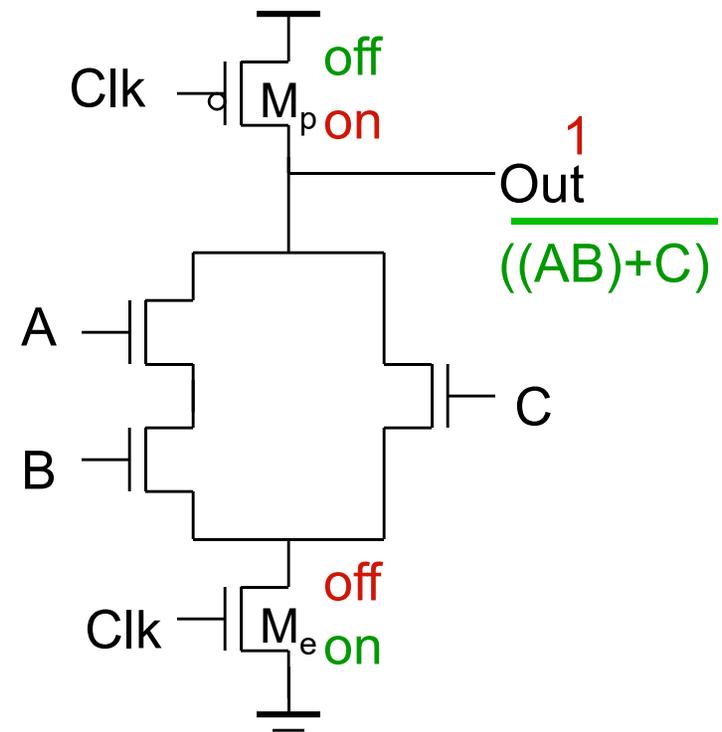
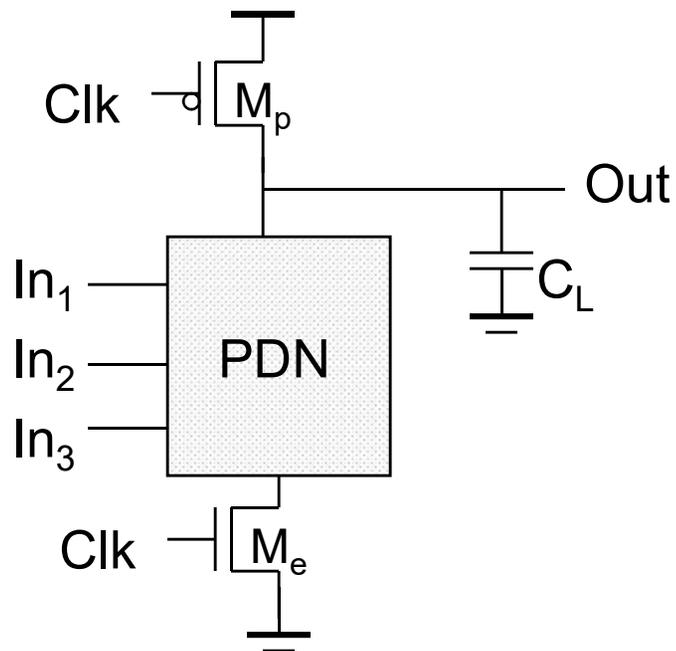


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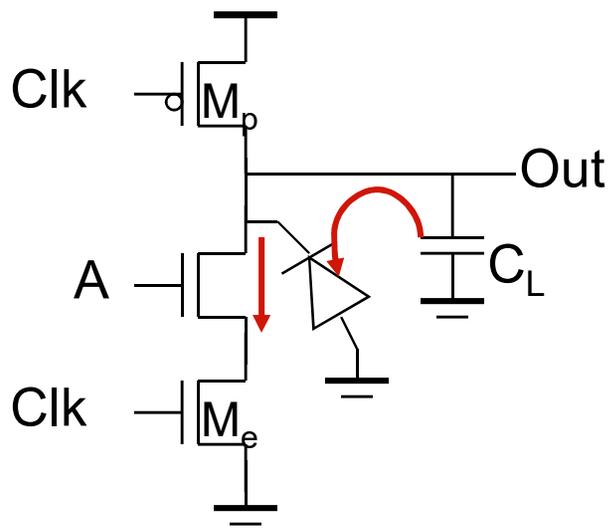
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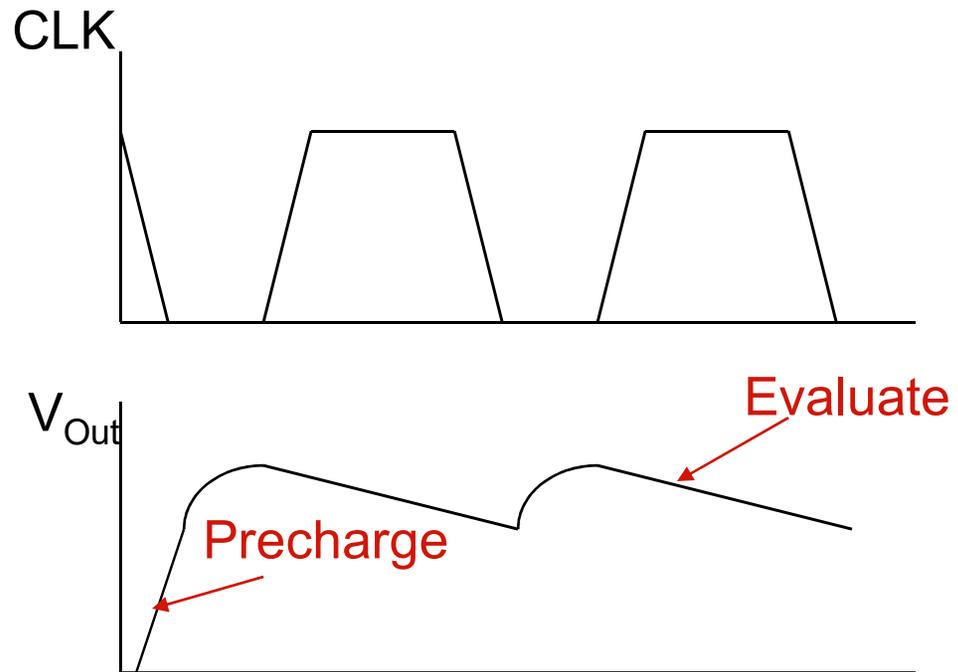
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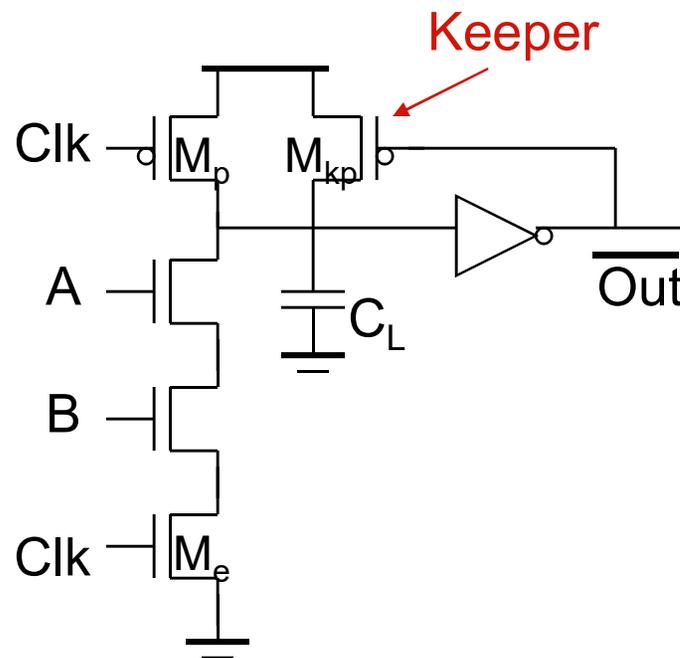


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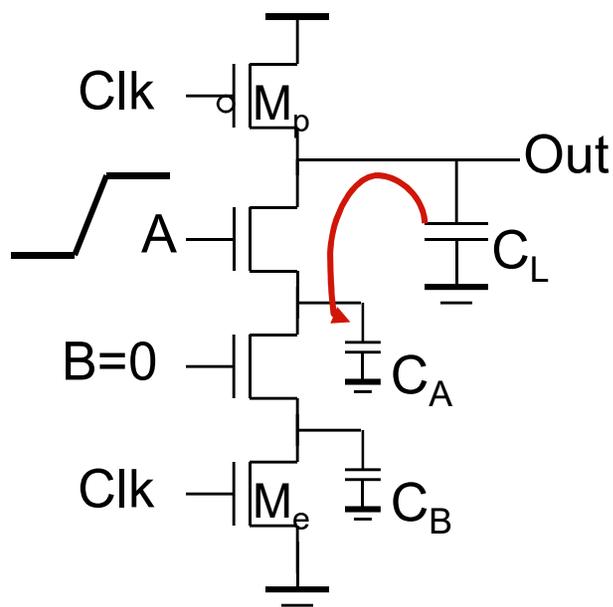
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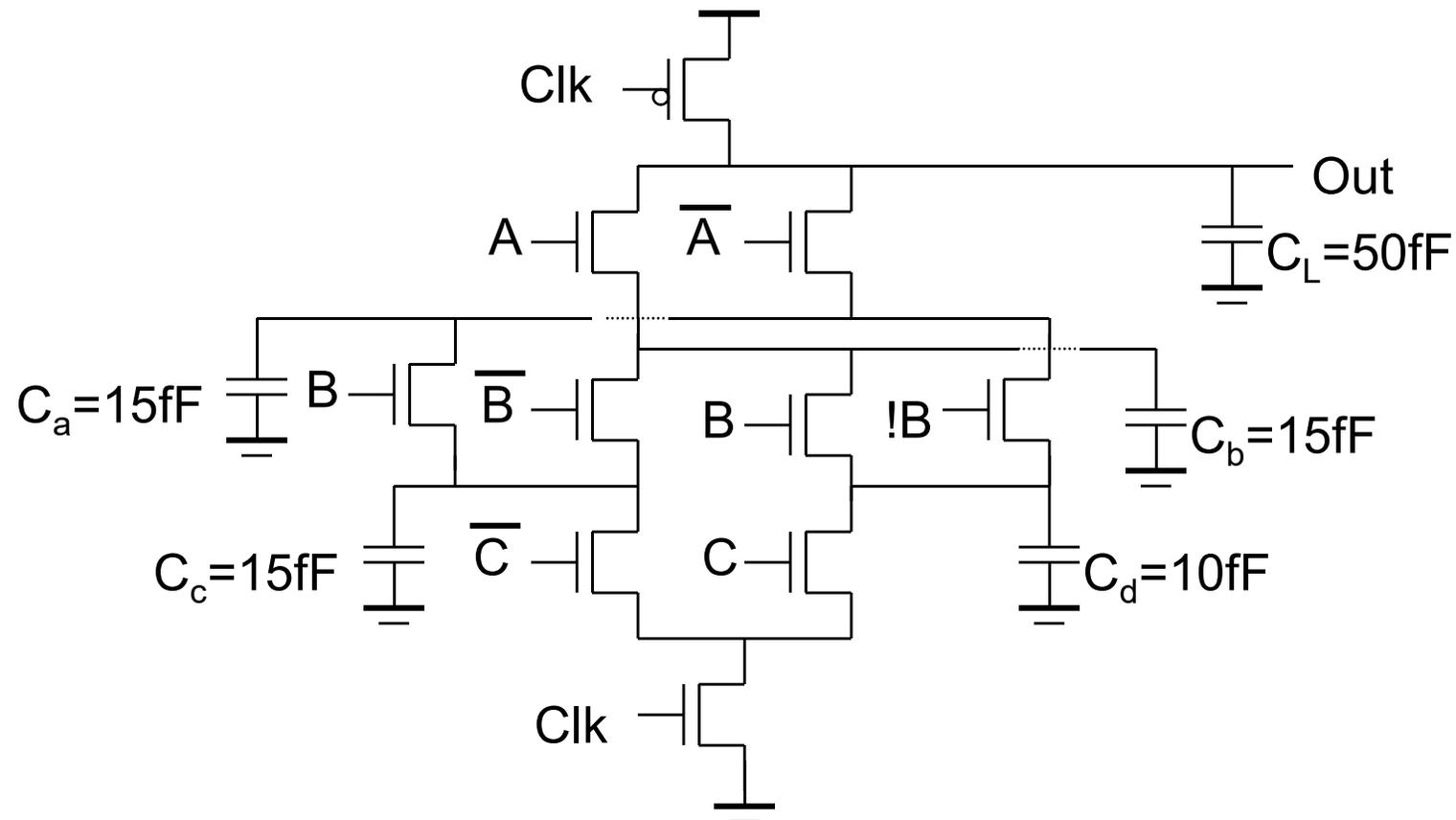
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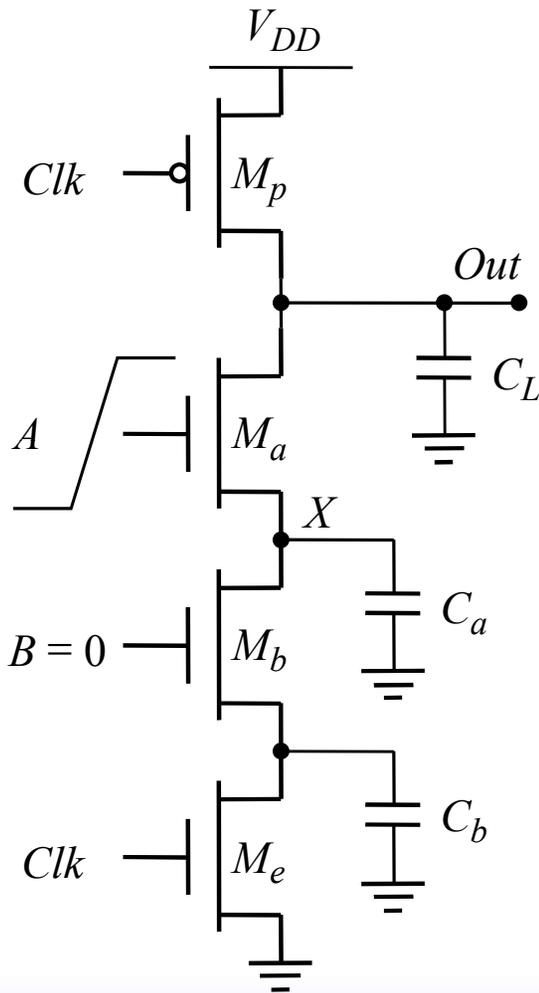


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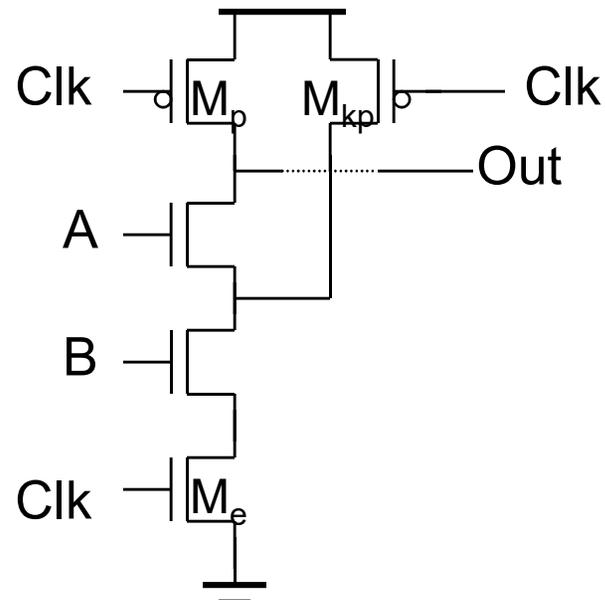
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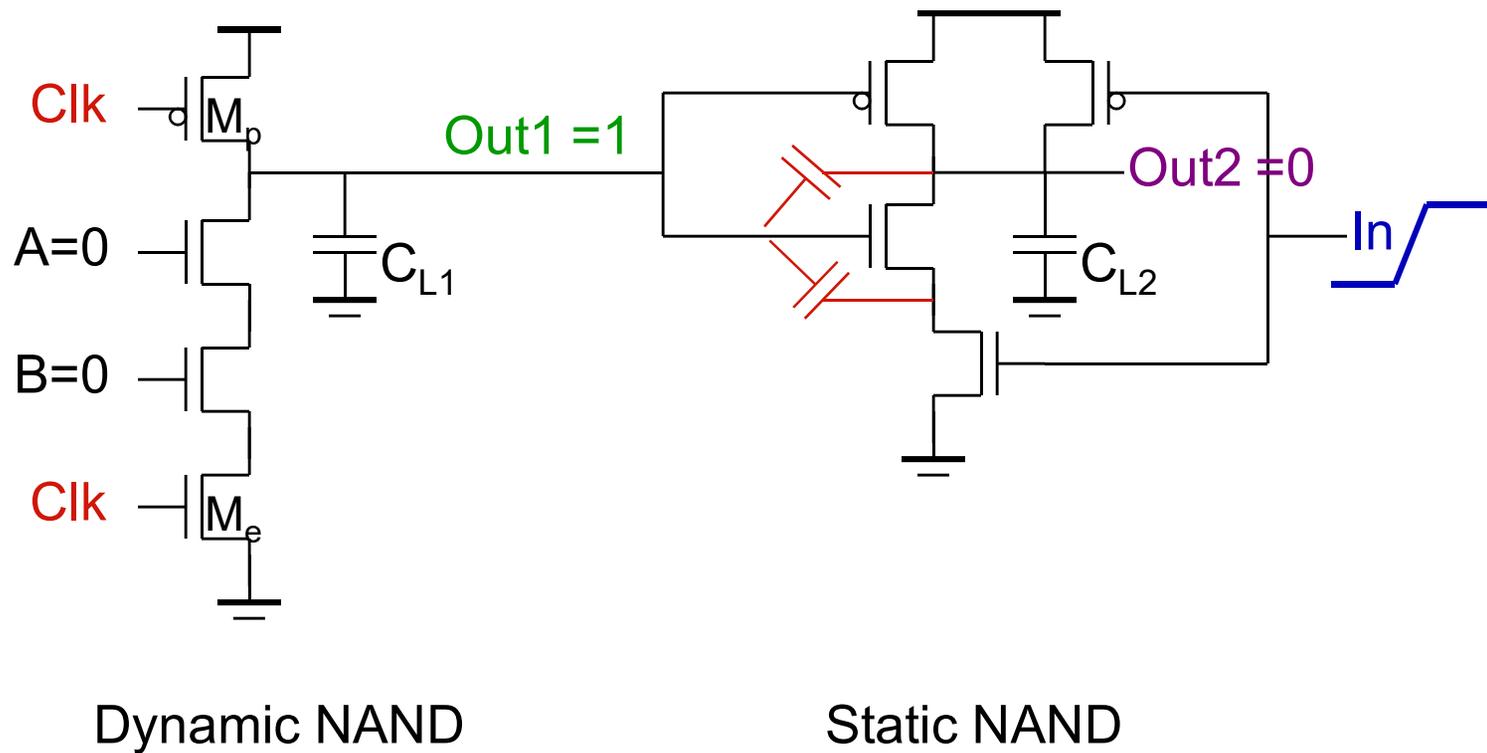
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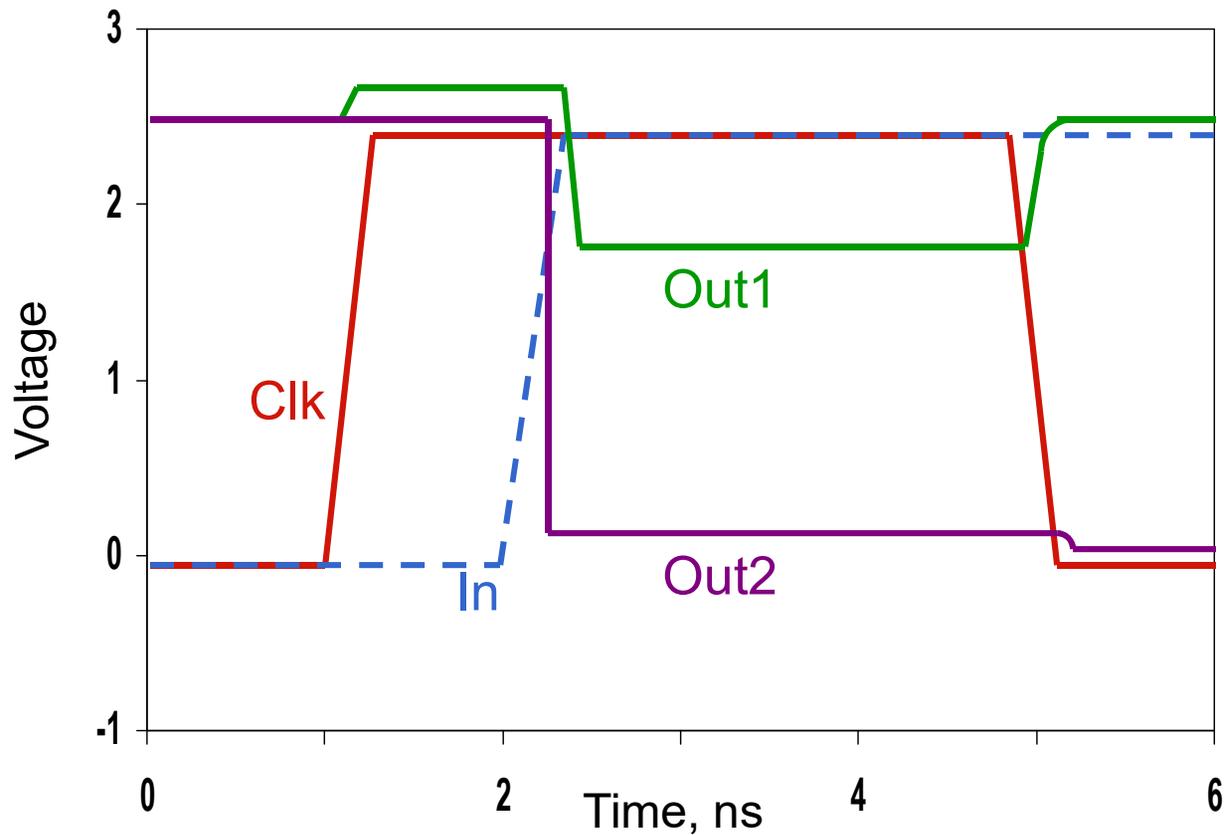


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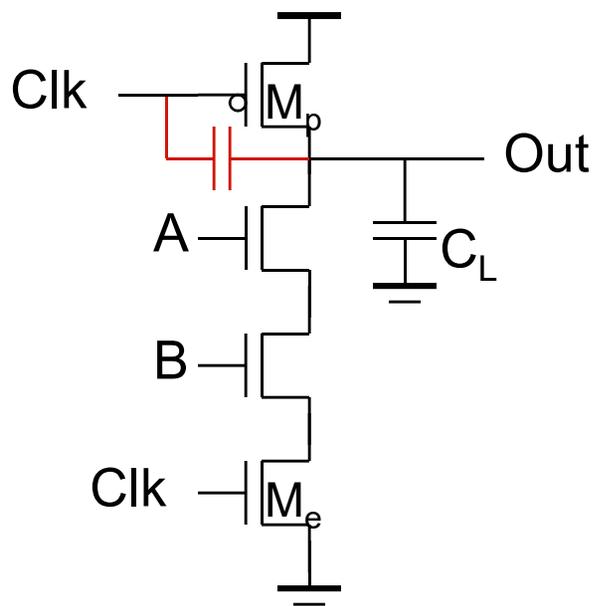
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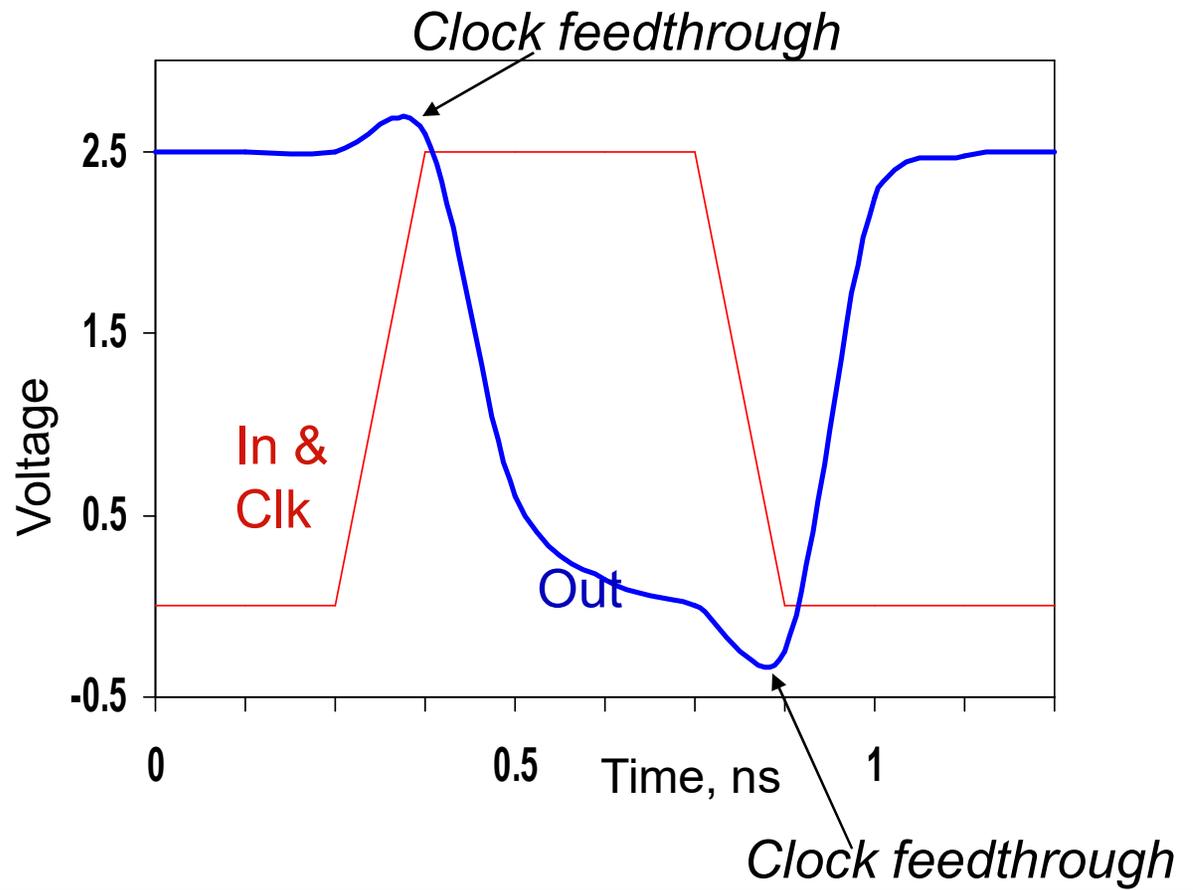
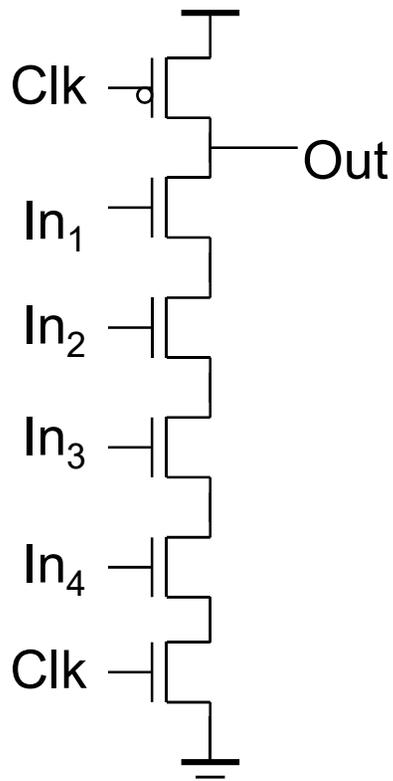


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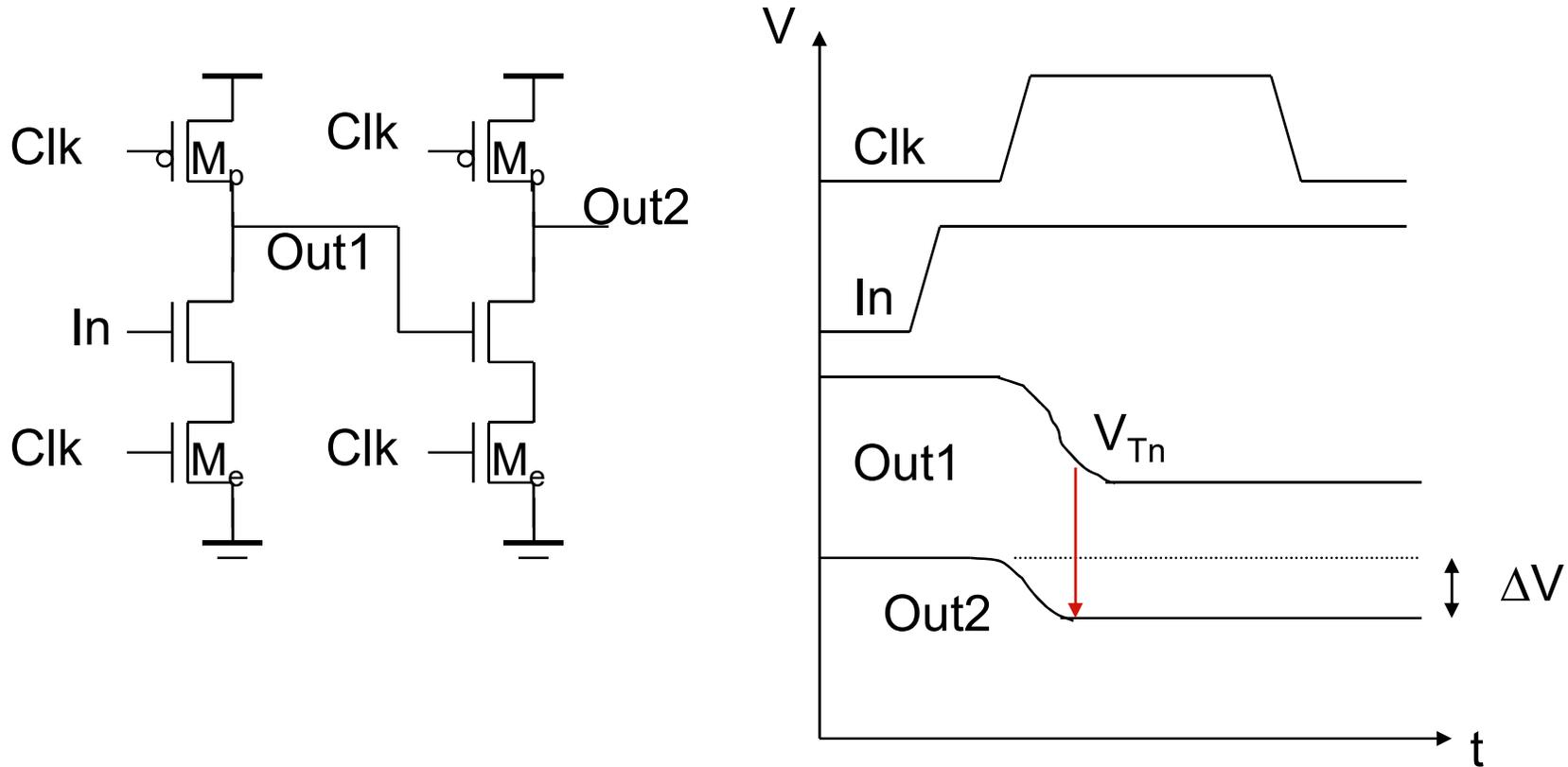
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