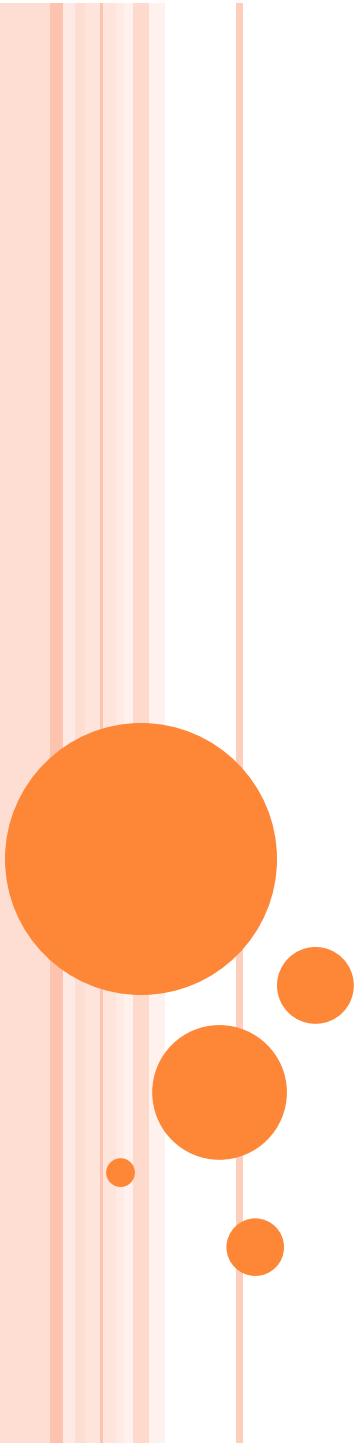


SoC Design Verification

Design for Verification

- Principle of **locality**
- **Plan** before design starts
- Testbenches should reflect the system environment
- Best strategy
  - Bottom-up verification
  - Challenges: developing testbench
  - Solution
    - Macros with clean, well-designed interface
    - High level verification languages + code coverage tool

System Interconnection

- Tri-state bus is not good
  - Bus contention problem
    - Reduce reliability
    - One and only one driver at a time
      - Harder for deep submicron design
  - Bus floating problem
    - Reduce reliability
    - Bus keeper
  - ATPG problem
  - FPGA prototyping problem
- **Multiplexer-based bus** is better

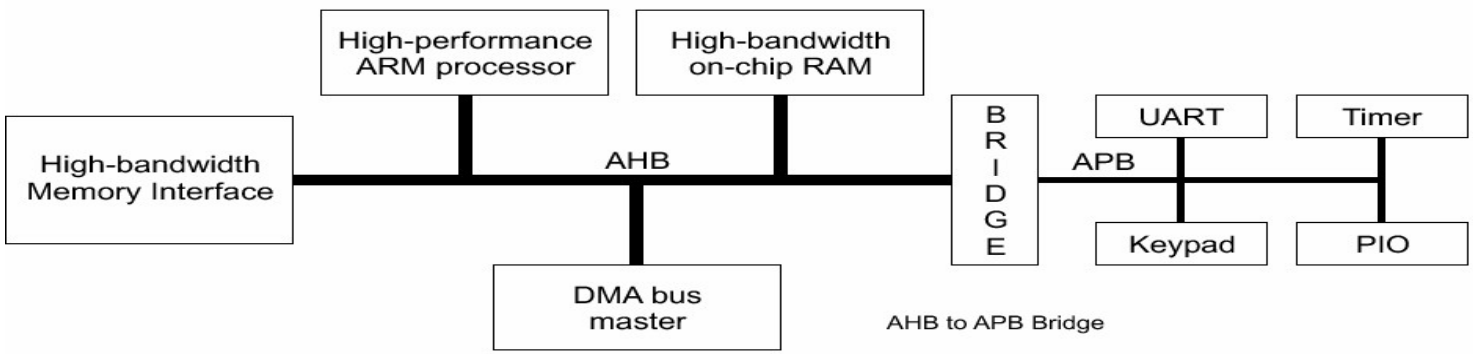
IP-TO-IP INTERFACE

- Direct connection (via FIFO)
  - Higher bandwidth
  - Redesign for different IP
  - Become unmanageable when the IP number increases
  - Only suitable for design connected to analog block, e.g. PHY
- **Bus-based**
  - Eliminate direct link
  - Layered approach can offer higher bandwidth
  - All IPs talk to bus only, thus only **IP-to-bus problem**
  - The mainstream of current IP-based SOC integration
- Choose the **standard bus** whenever possible

On-chip Bus (OCB)

- **ARM AMBA**
  - Advanced Microcontroller Bus Architecture
  - Dominant player
  - V 3.0 is on the road
  - Available solution
    - Synopsys DW_AMBA, …
- Sonics OCP
- VSIA OCB 2.1
- WishBone Silicore
- IBM CoreConnect

AMBA Bus System



AHB to APB Bridge

AMBA Advanced High-performance Bus (AHB)
* High performance
* Pipelined operation
* Burst transfers
* Multiple bus masters
* Split transactions

AMBA Advanced Peripheral Bus (APB)
* Low power
* Latched address and control
* Simple interface
* Suitable for many peripherals