



SoC SYSTEM INTERCONNECT

SYSTEM INTERCONNECTION

- Tri-state bus is not good
 - Bus contention problem
 - Reduce reliability
 - One and only one driver at a time
 - Harder for deep submicron design
 - Bus floating problem
 - Reduce reliability
 - Bus keeper
 - ATPG problem
 - FPGA prototyping problem
- **Multiplexer-based bus** is better



IP-TO-IP INTERFACE

- Direct connection (via FIFO)
 - Higher bandwidth
 - Redesign for different IP
 - Become unmanageable when the IP number increases
 - Only suitable for design connected to analog block, e.g. PHY
- **Bus-based**
 - Eliminate direct link
 - Layered approach can offer higher bandwidth
 - All IPs talk to bus only, thus only **IP-to-bus problem**
 - The mainstream of current IP-based SOC integration
- Choose the **standard bus** whenever possible

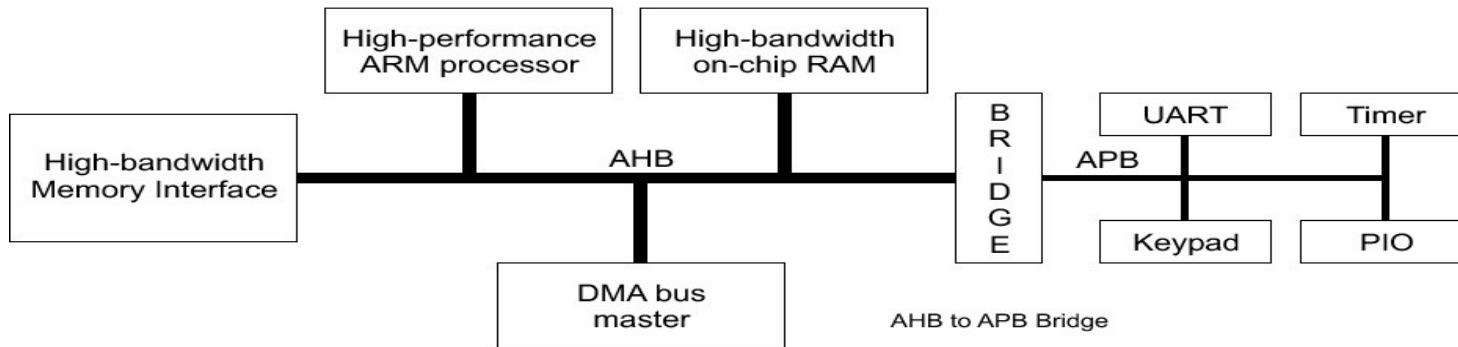


ON-CHIP BUS (OCB)

- **ARM AMBA**
 - Advanced Microcontroller Bus Architecture
 - Dominant player
 - V 3.0 is on the road
 - Available solution
 - Synopsys DW_AMBA, ...
- Sonics OCP
- VSIA OCB 2.1
- WishBone Silicore
- IBM CoreConnect



AMBA BUS SYSTEM



AMBA Advanced High-performance Bus (AHB)

- * High performance
- * Pipelined operation
- * Burst transfers
- * Multiple bus masters
- * Split transactions

AMBA Advanced Peripheral Bus (APB)

- * Low power
- * Latched address and control
- * Simple interface
- * Suitable for many peripherals



DESIGN FOR DEBUG: ON-CHIP DEBUG

- Experienced teams assume chip won't work when first power up and plan accordingly.
- Challenges for IP test
 - IPs are **deeply embedded** within the SOC design
 - Disaster to the system and S/W engineers
- Solution
 - Principle: increase **controllability and observability**
 - Add debug support logic to the hardware
 - MUX bus to existing I/O pins



LOW POWER (1/3)

$$P = \sum \alpha C V^2 f$$

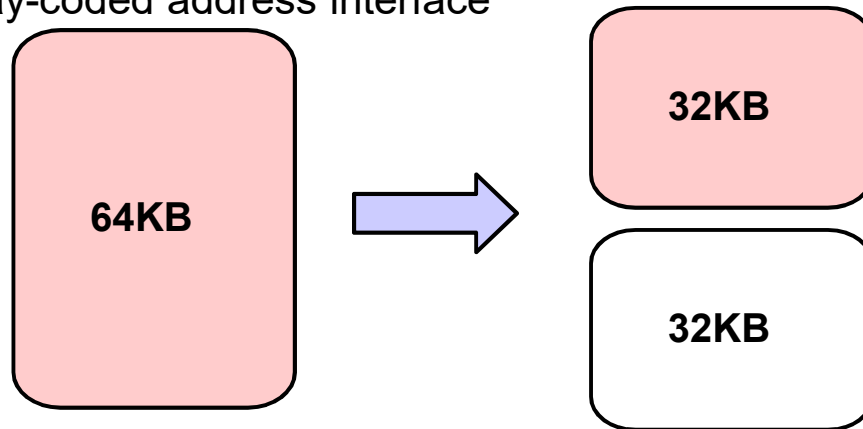
α : switching activity, C : capacitance, V : supply voltage, f : frequency

- Reduce the supply voltage
 - Process improvement
- Reduce capacitance
 - Low power cell and I/O library
 - Less logic for the same performance
- Reduce switching activity
 - Architecture and RTL exploration
 - Power-driven synthesis
 - Gate-level power optimization



LOW POWER (2/3)

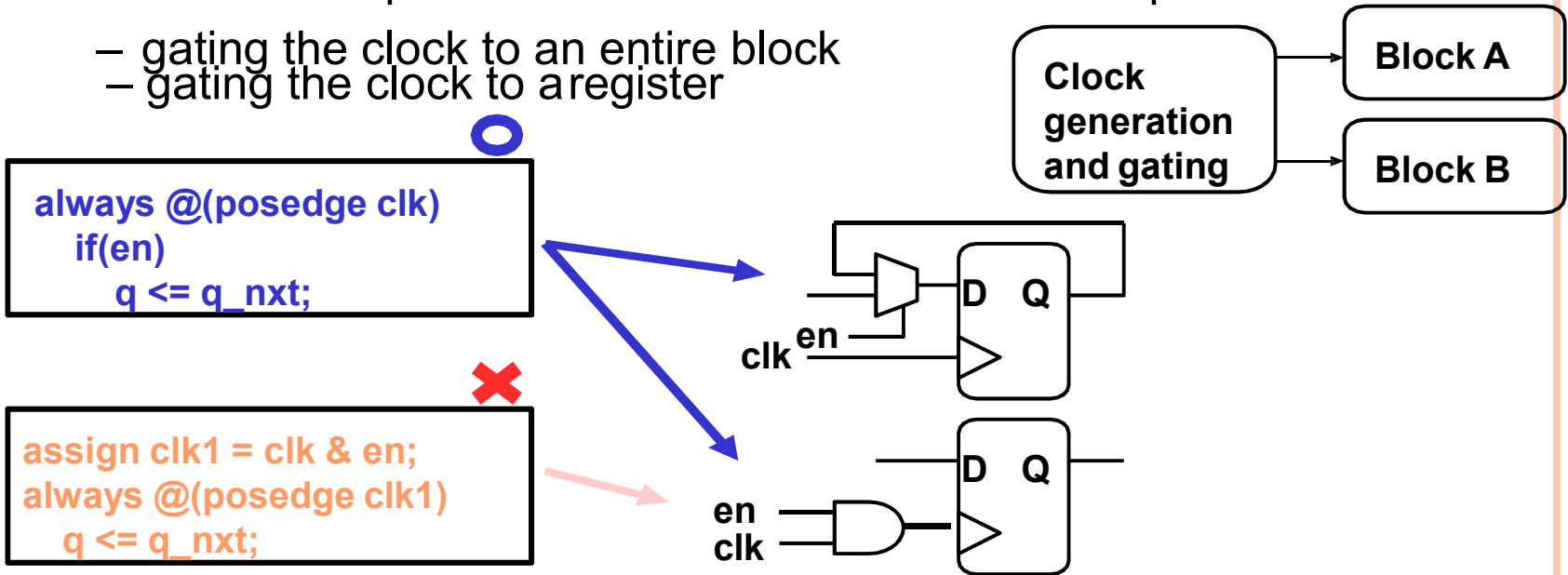
- Memory
 - Dominated power consumption
 - Low-power memory circuit design
 - Partition a large memory into several small blocks
 - Gray-coded address interface



LOW POWER (3/3)

- **Clock gating**

- 50% - 70% power consumed in clock network reported
- gating the clock to an entire block
- gating the clock to a register



DESIGN FOR TEST

- Memory test
 - Memory BIST is recommended
- Processor test
 - Chip level test controller (including scan chain controller and JTAG controller)
 - Use shadow registers to facilitate full-scan testing of boundary logic
- Other macros
 - **Full scan** is strongly recommended
- Logic BIST
 - Embedded stimulus generator and response checker
 - Not popular yet

