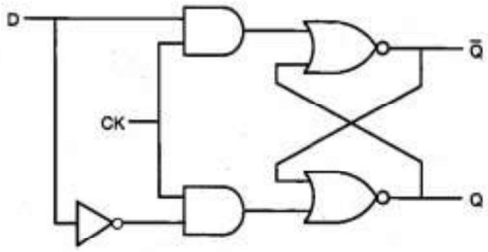
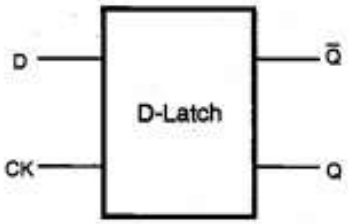
CMOS D-Latch and Edge – Triggered Flip-Flop

- Gate-level schematic that the output Q assumes the value of the input D when the clock is active, i.e., for CK = "1.“
- When the clock signal goes to zero, the output will simply preserve its state. Thus, the CK input acts as an enable signal which allows data to be accepted into the D-latch.
- Used for temporary storage of data or as a delay element.

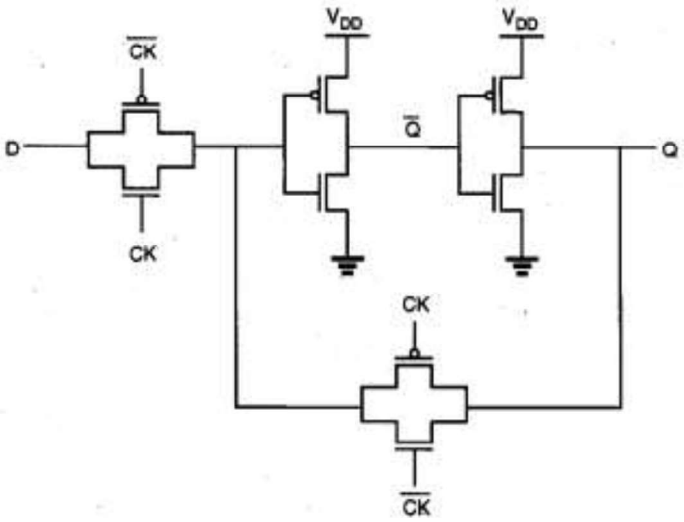


Gate level schematic view of the D-Latch



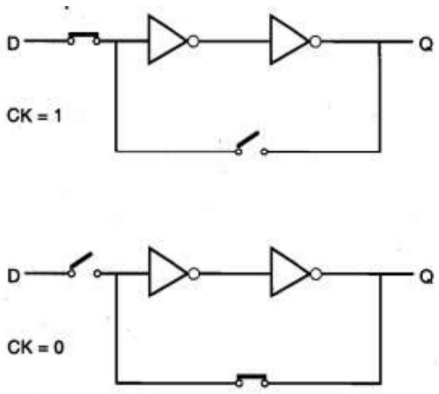
Block diagram view of the D-Latch

- The TG at the input is activated by the CK signal, whereas the TG in the inverter loop is activated by the inverse of the CK signal, CK.
- Thus, the input signal is accepted (latched) into the circuit when the clock is high, and this information is preserved as the state of the inverter loop when the clock is low.
- The operation of the CMOS D-latch circuit can be better visualized by replacing the CMOS transmission gates with simple switches

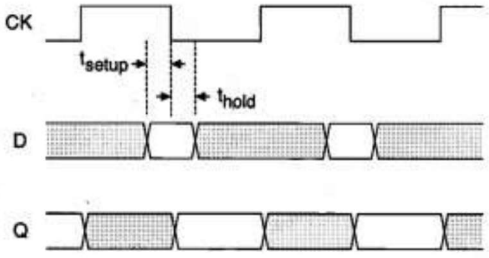


CMOS implementation of the D-Latch

- D input must be stable for a short time before (setup time, tsetup) and after (hold time, thold) the negative clock transition, during which the input switch opens and the loop switch closes.
- Once the inverter loop is completed by closing the loop switch, the output will preserve its valid level.
- In the D-latch design, the requirements for setup time and hold time should be met carefully.
- Any violation of such specifications can cause metastability problems which lead to seemingly chaotic transient behavior, and can result in an unpredictable state after the transitional period.
- The transparency property makes the application of this D-latch unsuitable for counters and some data storage implementations.



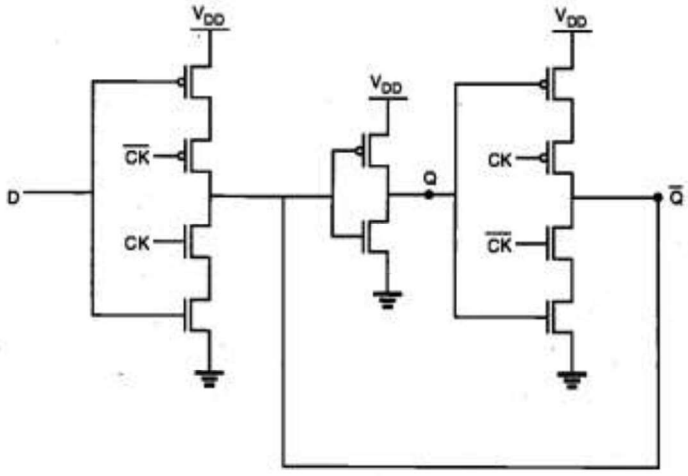
Simplified schematic view



Timing diagram of the CMOS D-Latch

D Flip-flop with Tristate inverter

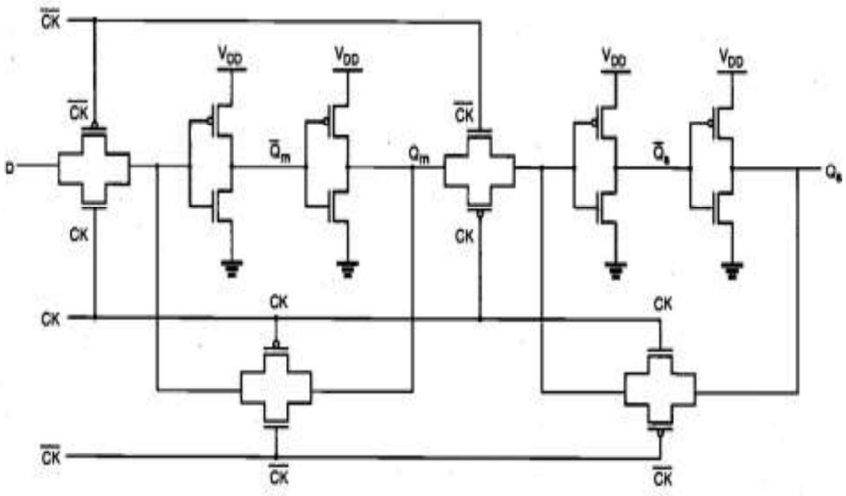
- The first tri-state inverter acts as the input switch, accepting the input signal when the clock is high.
- At this time, the second tristate inverter is at its high-impedance state, and the output Q is following the input signal.
- When the clock goes low, the input buffer becomes inactive, and the second tristate inverter completes the two-inverter loop, which preserves its state until the next clock pulse.



CMOS implementation of D-Latch

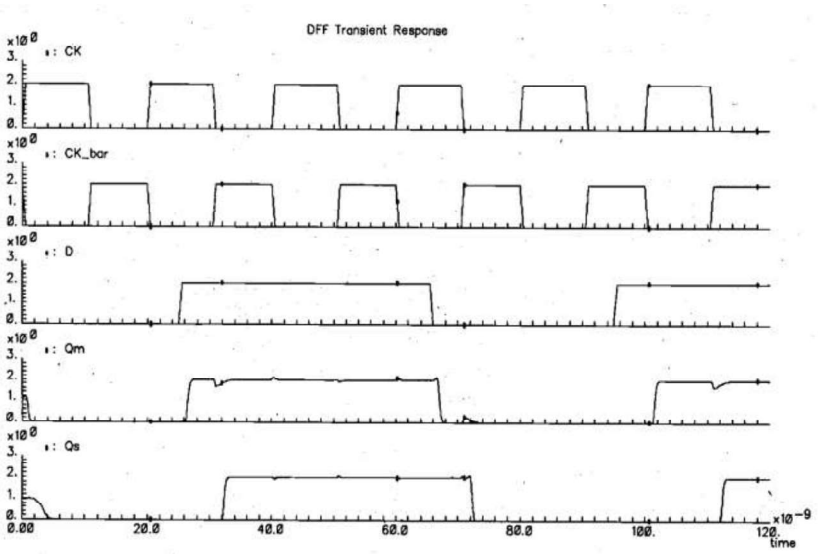
Master–Slave D Flip-flop

- The two-stage master-slave flip-flop circuit shown in Fig, which is constructed by simply cascading two, D-latch circuits.
- The first stage (master) is driven by the clock signal, while the second stage (slave) is driven by the inverted clock signal.
- Thus, the master stage is positive level-sensitive, while the slave stage is negative level-sensitive.
- When the clock is, high, the master stage follows the D input while the slave stage holds the previous value.
- When the clock changes from logic "1" to logic “0" the master latch ceases to sample the input and stores the D value at the time of the clock transition.

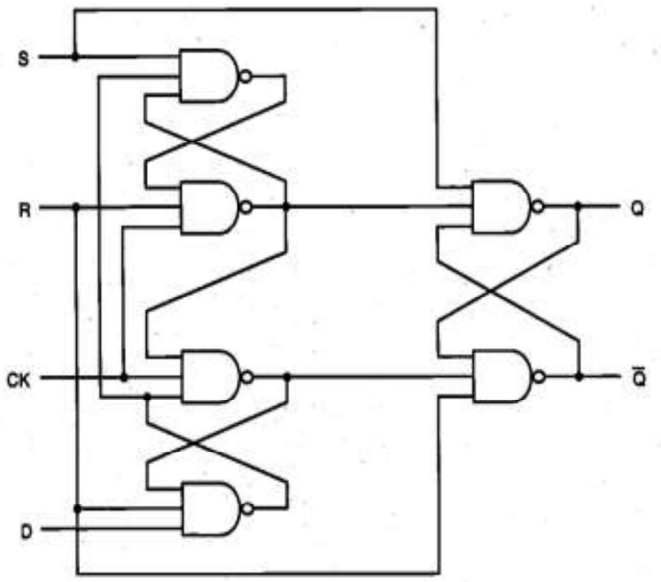


CMOS negative edge-triggered master – slave DFF

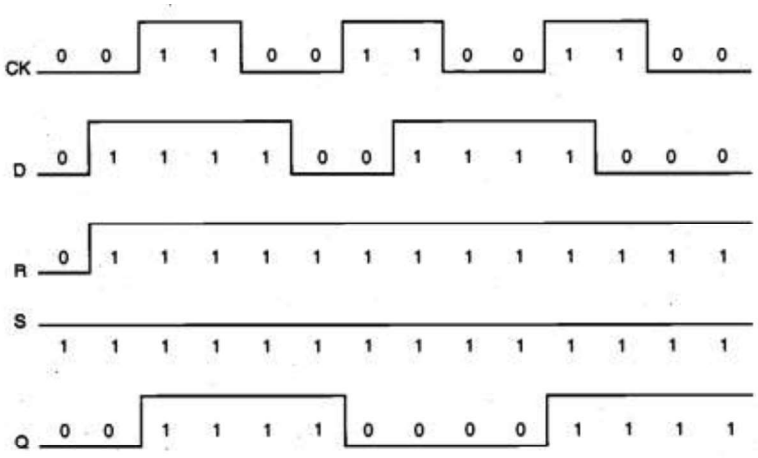
- At the same time, the slave latch becomes transparent, passing the stored master value Qm to the output of the slave stage, Qs.
- The input cannot affect the output because the master stage is disconnected from the D input.
- When the clock changes again from logic 0" to 1," the slave latch locks in the master latch output and the master stage starts sampling the input again.



Output waveform of the CMOS DFF



NAND based positive edge DFF



Timing diagram of the positive edge-triggerd DFF

THANK YOU