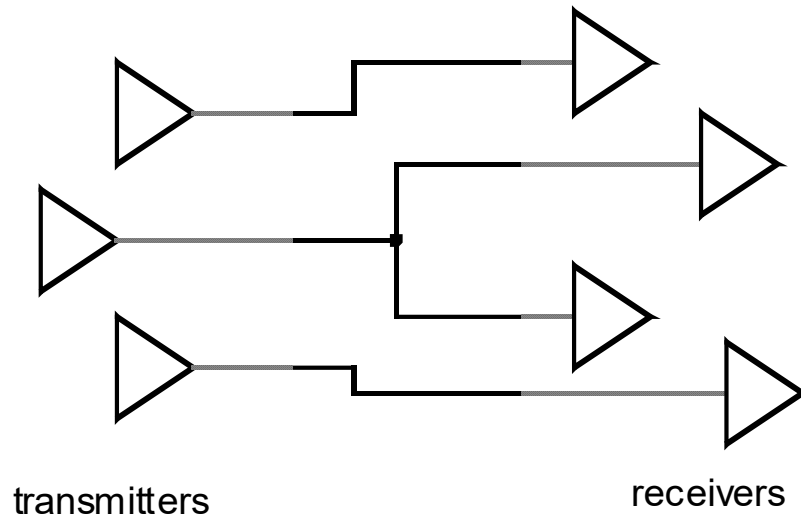


# The Wire

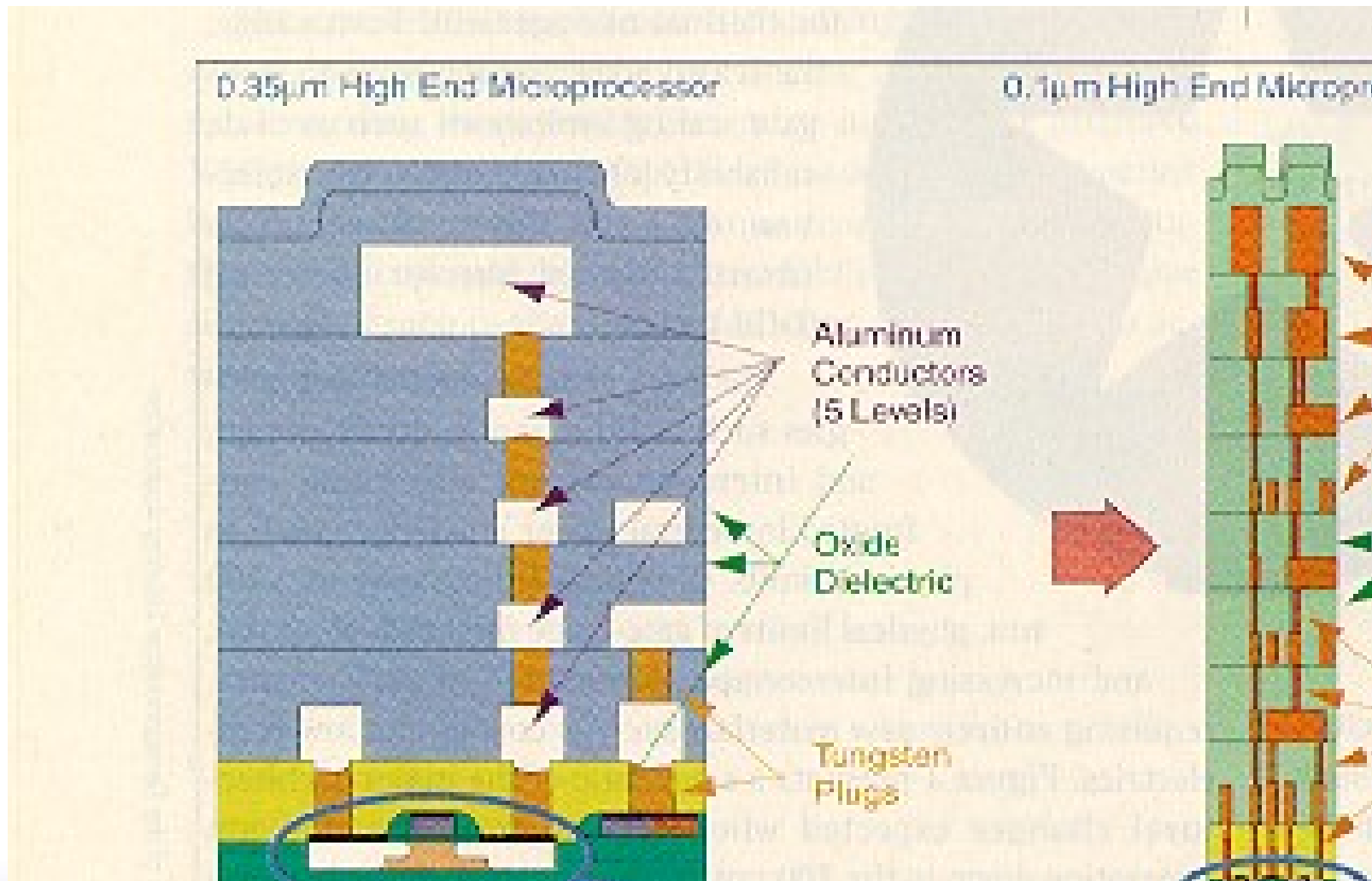


**schematics**

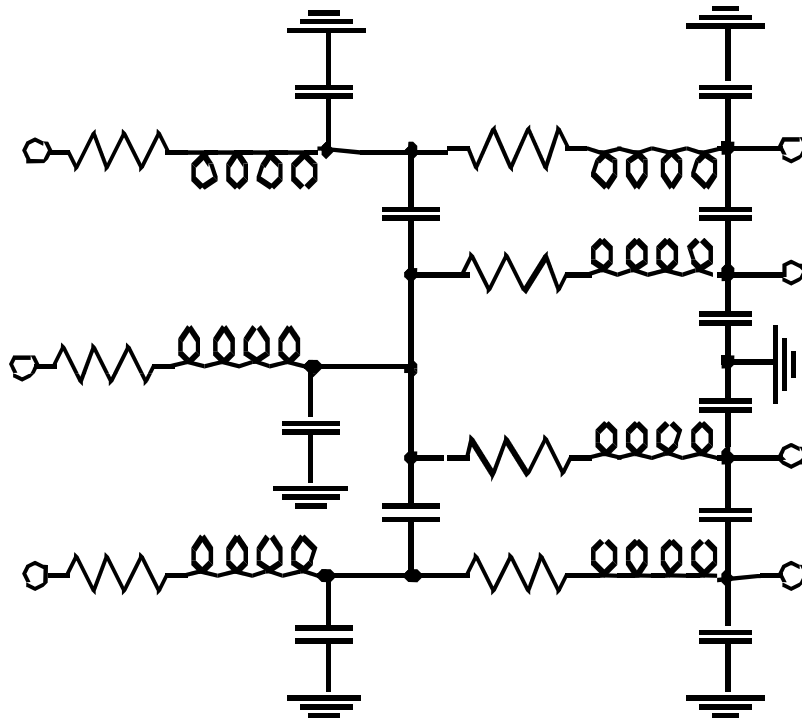


**physical**

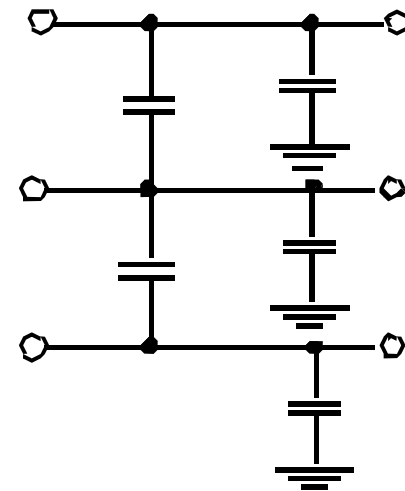
# Interconnect Impact on Chip



# Wire Models



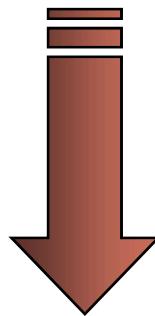
All-inclusive model



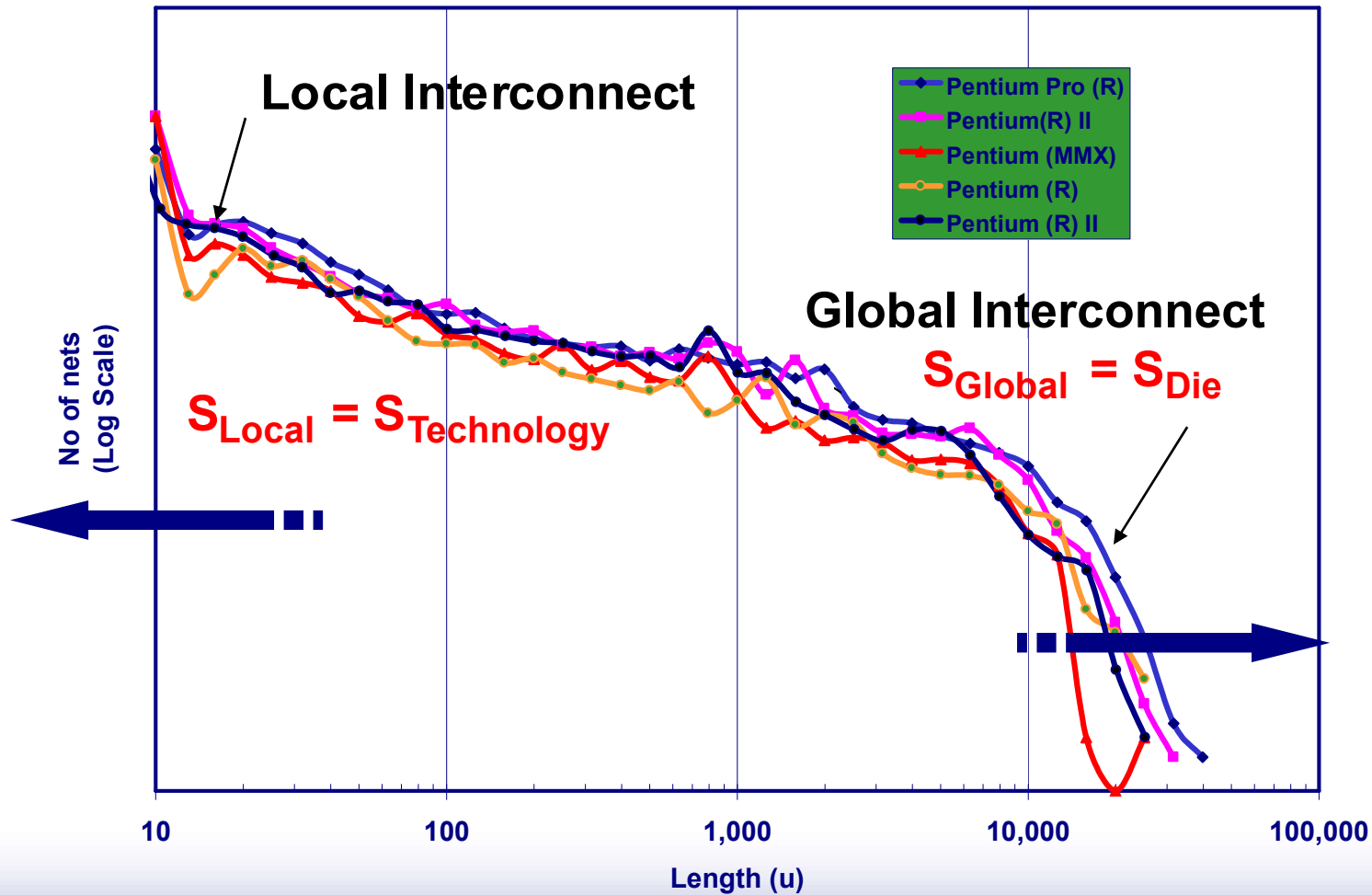
Capacitance-only

# *Impact of Interconnect Parasitics*

- Interconnect parasitics
  - reduce reliability
  - affect performance and power consumption
- Classes of parasitics
  - Capacitive
  - Resistive
  - Inductive



# Nature of Interconnect



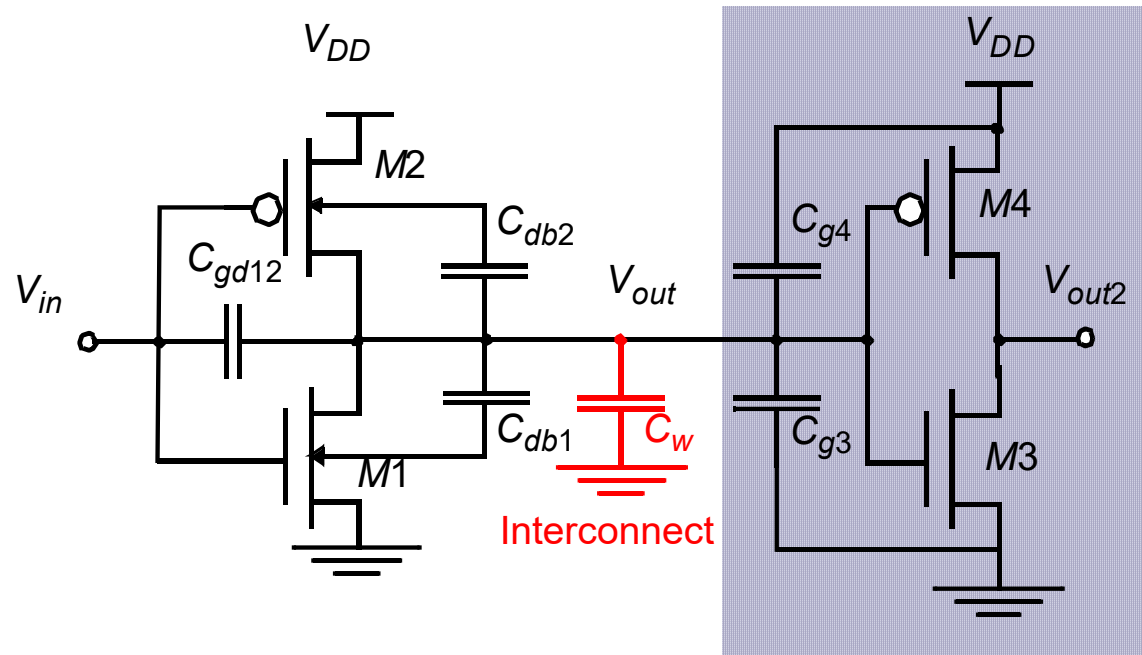
Source: Intel

# INTERCONNECT

Capacitance

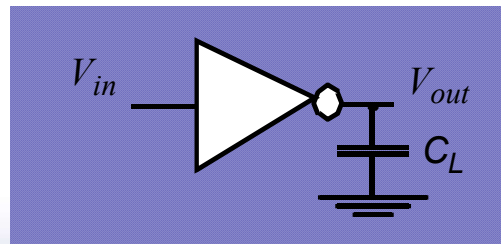


# Capacitance of Wire Interconnect

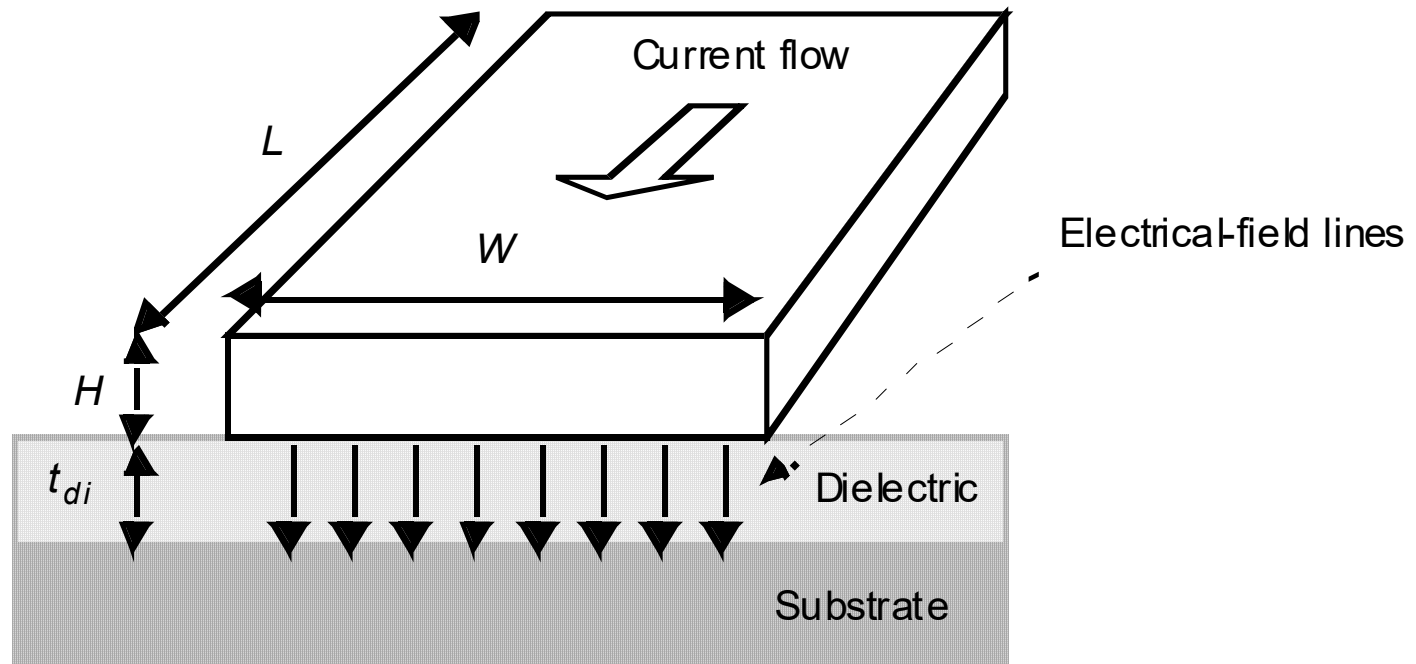


Fanout

Simplified Model



# Capacitance: The Parallel Plate Model



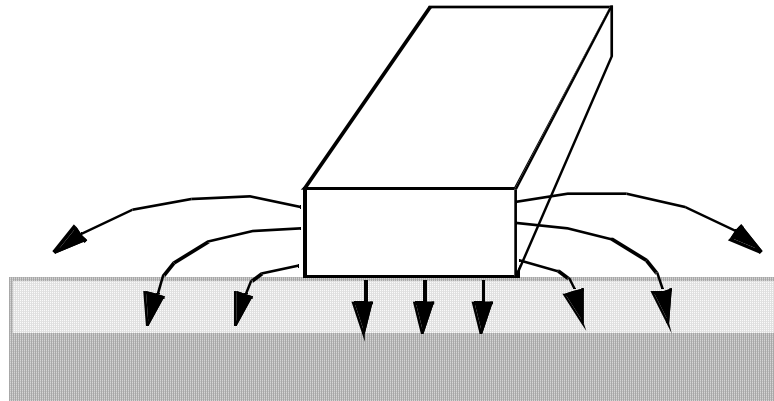
$$C_{int} = \frac{\epsilon_{di}}{t_{di}} WL$$

$$S_{Cwire} = \frac{S}{S \cdot S_L} = \frac{1}{S_L}$$

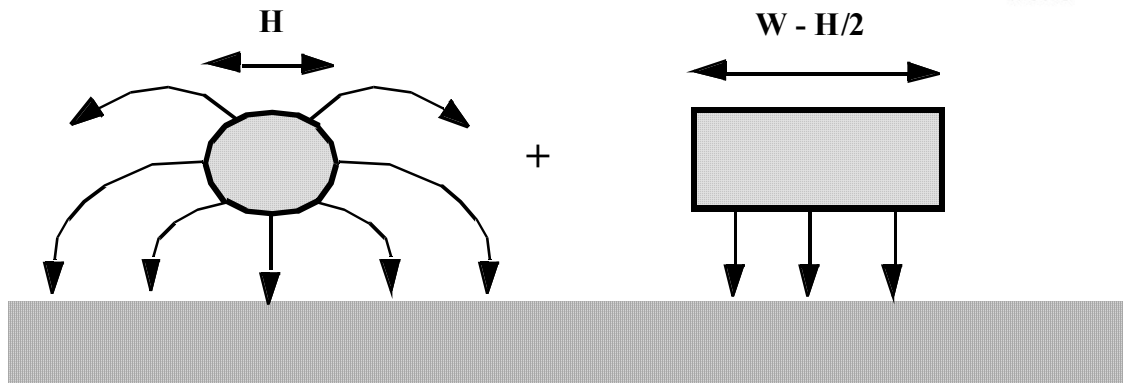
# Permittivity

Material	$\epsilon_r$
Free space	1
Aerogels	~1.5
Polyimides (organic)	3-4
Silicon dioxide	3.9
Glass-epoxy (PC board)	5
Silicon Nitride ( $\text{Si}_3\text{N}_4$ )	7.5
Alumina (package)	9.5
Silicon	11.7

# Fringing Capacitance



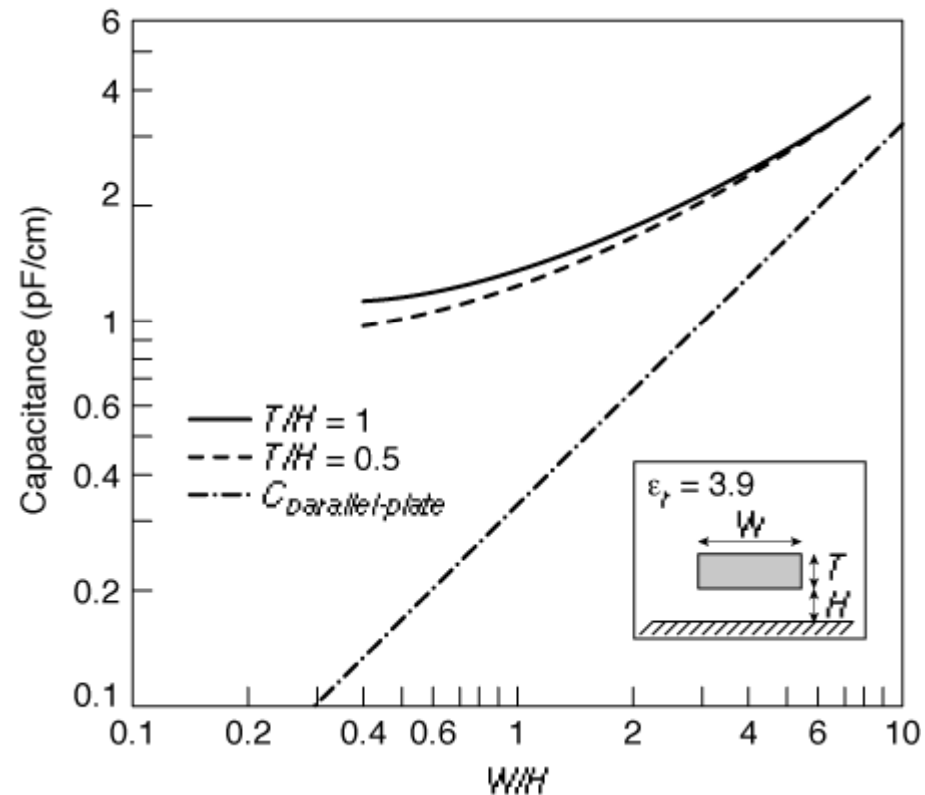
(a)



(b)

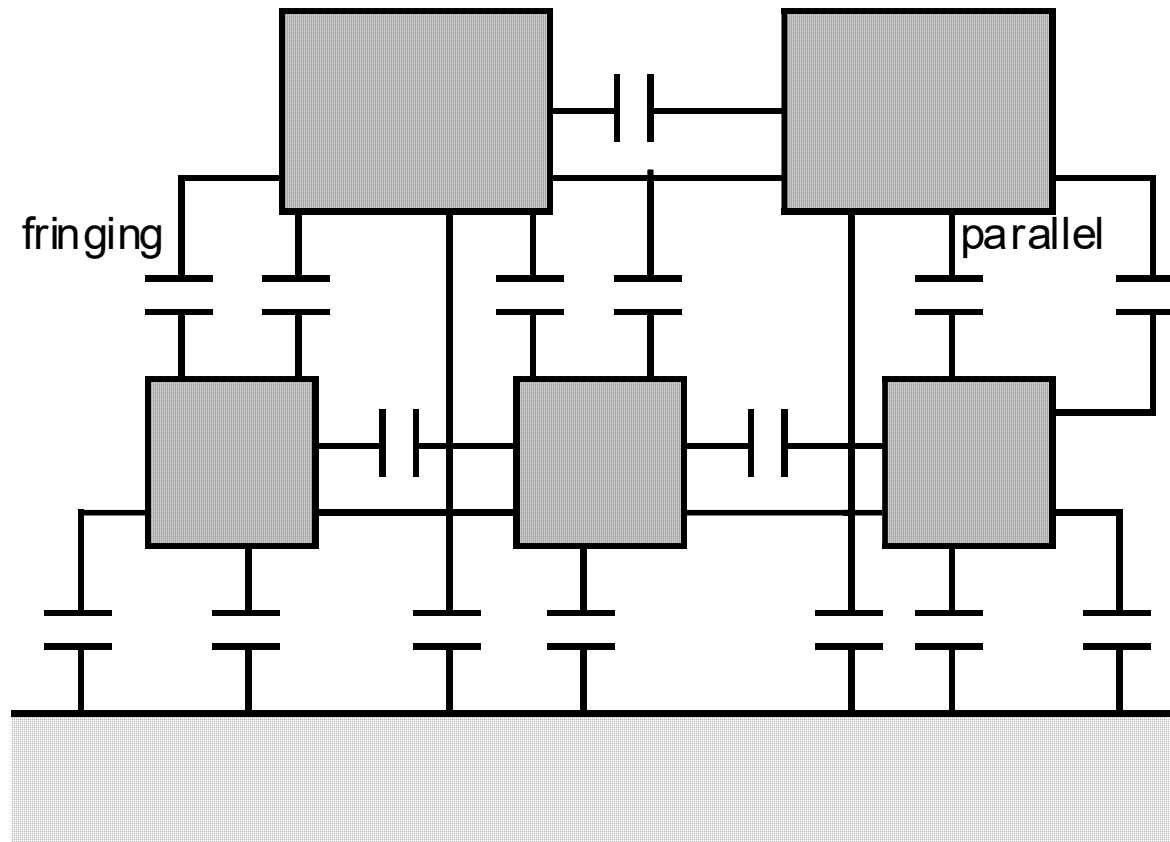
$$C_{wire} = C_{pp} + C_{fringe} = \frac{w\epsilon_{di}}{t_{di}} + \frac{2\pi\epsilon_{di}}{\log(t_{di}/H)}$$

# Fringing versus Parallel Plate

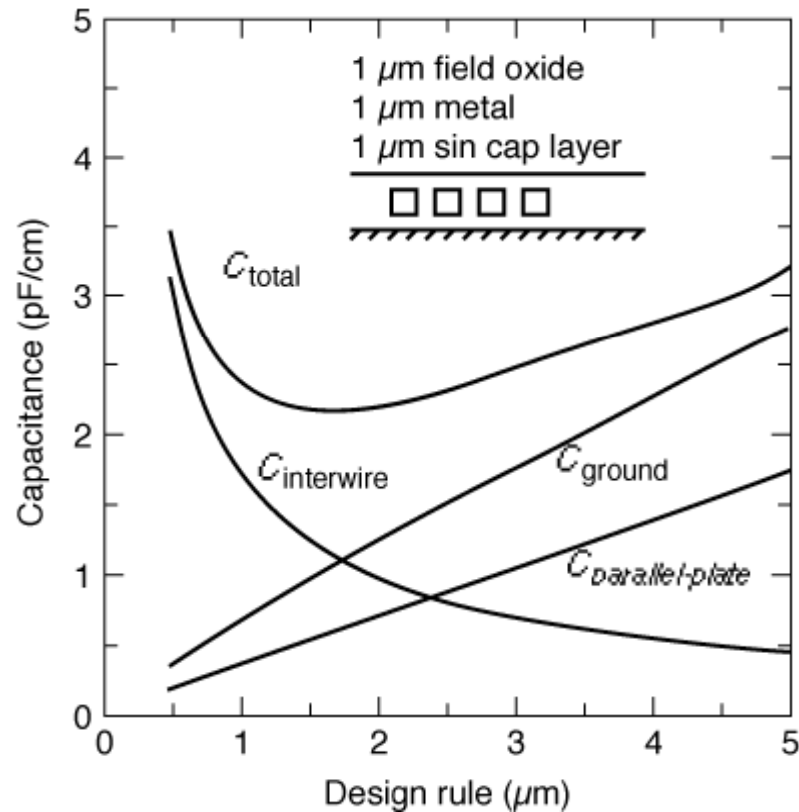


(from [Bakoglu89])

# Interwire Capacitance



# Impact of Interwire Capacitance



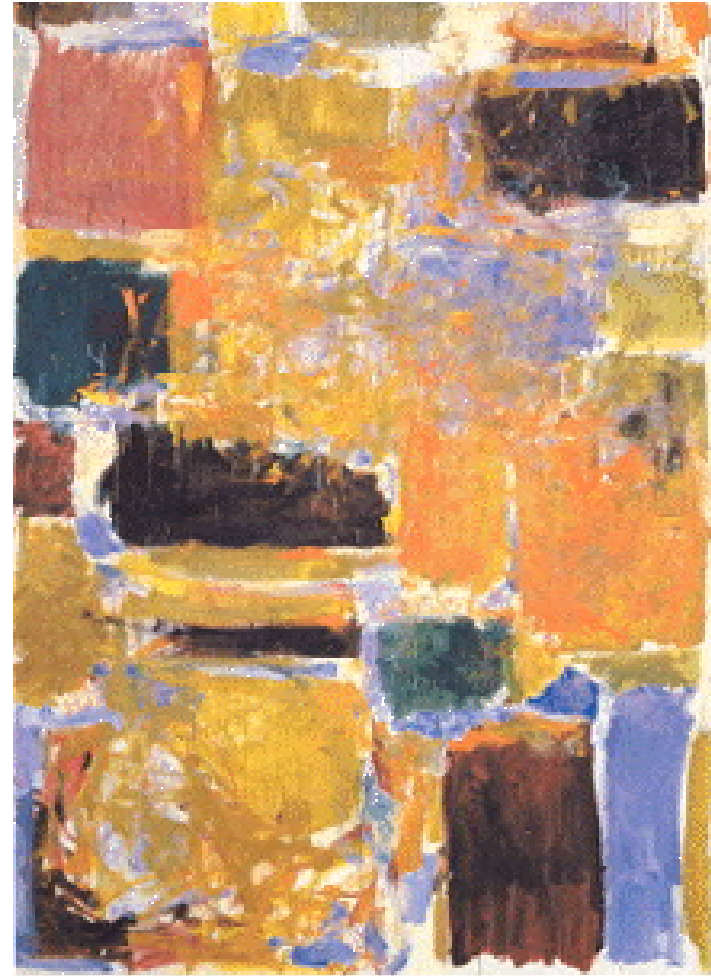
(from [Bakoglu89])

# Wiring Capacitances (0.25 $\mu\text{m}$ CMOS)

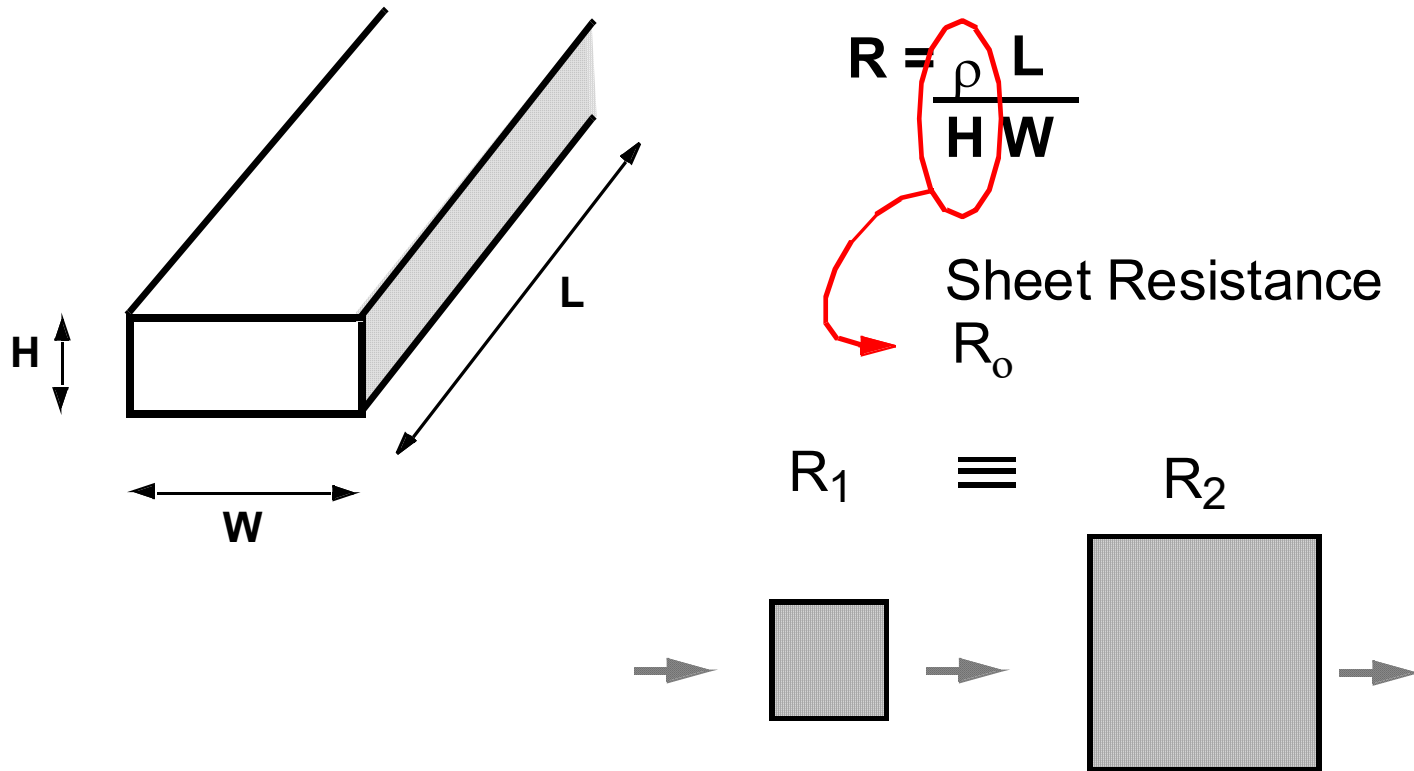
	Field	Active	Poly	Al1	Al2	Al3	Al4
Poly	88						
	54						
Al1	30	41	57				
	40	47	54				
Al2	13	15	17	36			
	25	27	29	45			
Al3	8.9	9.4	10	15	41		
	18	19	20	27	49		
Al4	6.5	6.8	7	8.9	15	35	
	14	15	15	18	27	45	
Al5	5.2	5.4	5.4	6.6	9.1	14	38
	12	12	12	14	19	27	52

# INTERCONNECT

**Resistance**



# Wire Resistance



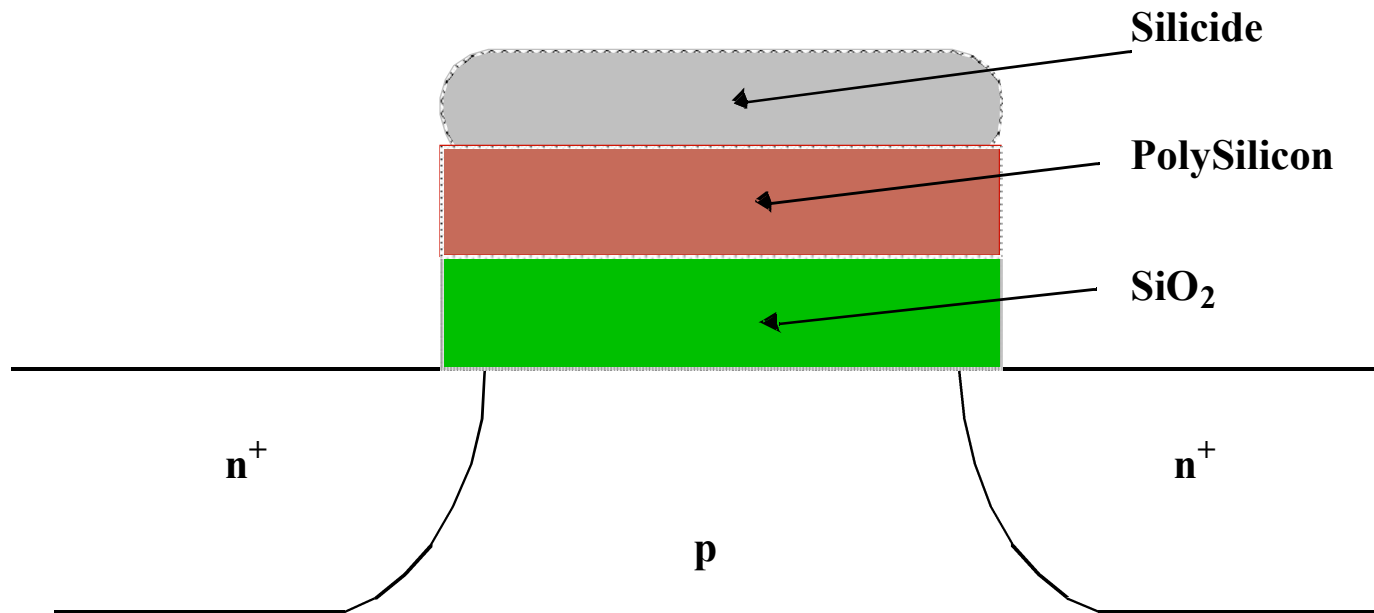
# Interconnect Resistance

<b>Material</b>	$\rho$ ( $\Omega\text{-m}$ )
Silver (Ag)	$1.6 \times 10^{-8}$
Copper (Cu)	$1.7 \times 10^{-8}$
Gold (Au)	$2.2 \times 10^{-8}$
Aluminum (Al)	$2.7 \times 10^{-8}$
Tungsten (W)	$5.5 \times 10^{-8}$

# *Dealing with Resistance*

- ❑ **Selective Technology Scaling**
- ❑ **Use Better Interconnect Materials**
  - reduce average wire-length
  - e.g. copper, silicides
- ❑ **More Interconnect Layers**
  - reduce average wire-length

# Polycide Gate MOSFET



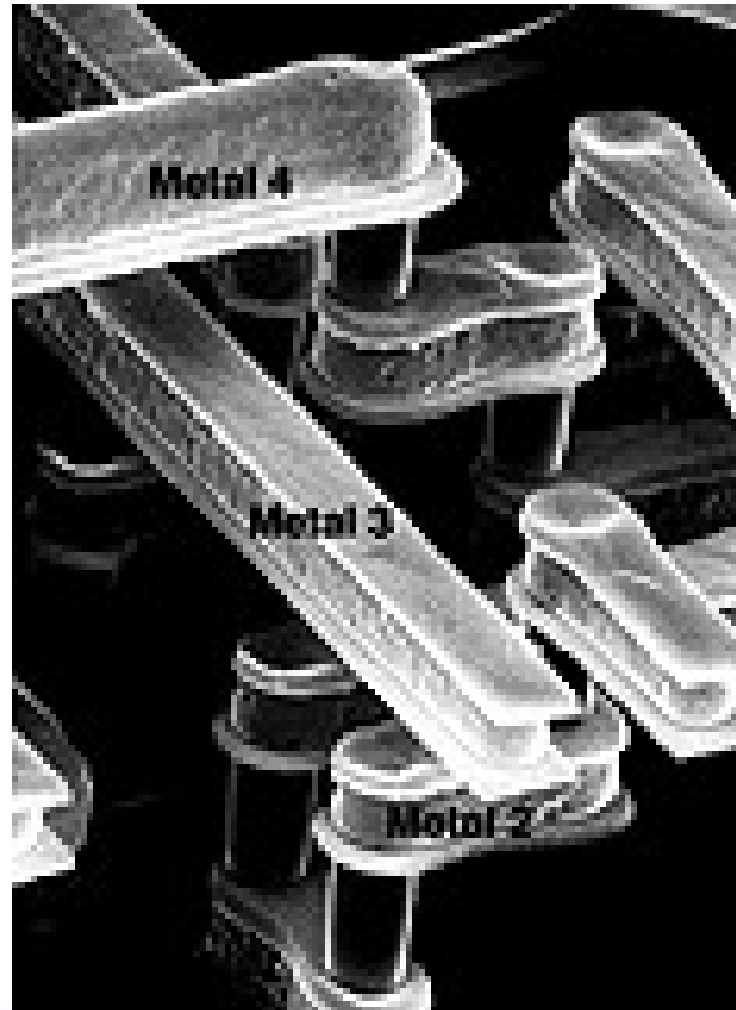
Silicides: WSi<sub>2</sub>, TiSi<sub>2</sub>, PtSi<sub>2</sub> and TaSi

Conductivity: 8-10 times better than Poly

# Sheet Resistance

Material	Sheet Resistance ( $\Omega/\square$ )
n- or p-well diffusion	1000 – 1500
$n^+$ , $p^+$ diffusion	50 – 150
$n^+$ , $p^+$ diffusion with silicide	3 – 5
$n^+$ , $p^+$ polysilicon	150 – 200
$n^+$ , $p^+$ polysilicon with silicide	4 – 5
Aluminum	0.05 – 0.1

# *Modern Interconnect*

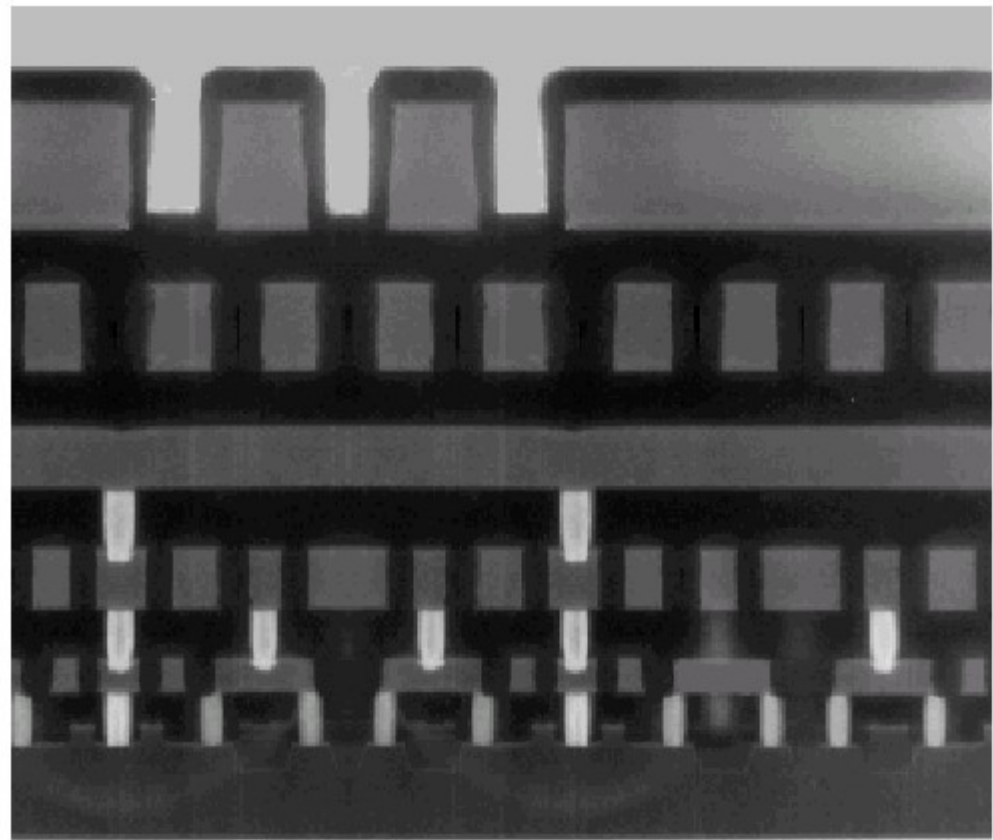


# Example: Intel 0.25 micron Process

5 metal layers  
Ti/Al - Cu/Ti/TiN  
Polysilicon dielectric

<u>LAYER</u>	<u>PITCH</u>	<u>THICK</u>	<u>A.R.</u>
Isolation	0.67	0.40	-
Polysilicon	0.64	0.25	-
Metal 1	0.64	0.48	1.5
Metal 2	0.93	0.90	1.9
Metal 3	0.93	0.90	1.9
Metal 4	1.60	1.33	1.7
Metal 5	2.56	1.90	1.5
	$\mu\text{m}$	$\mu\text{m}$	

Layer pitch, thickness and aspect ratio



# INTERCONNECT

**Inductance**

