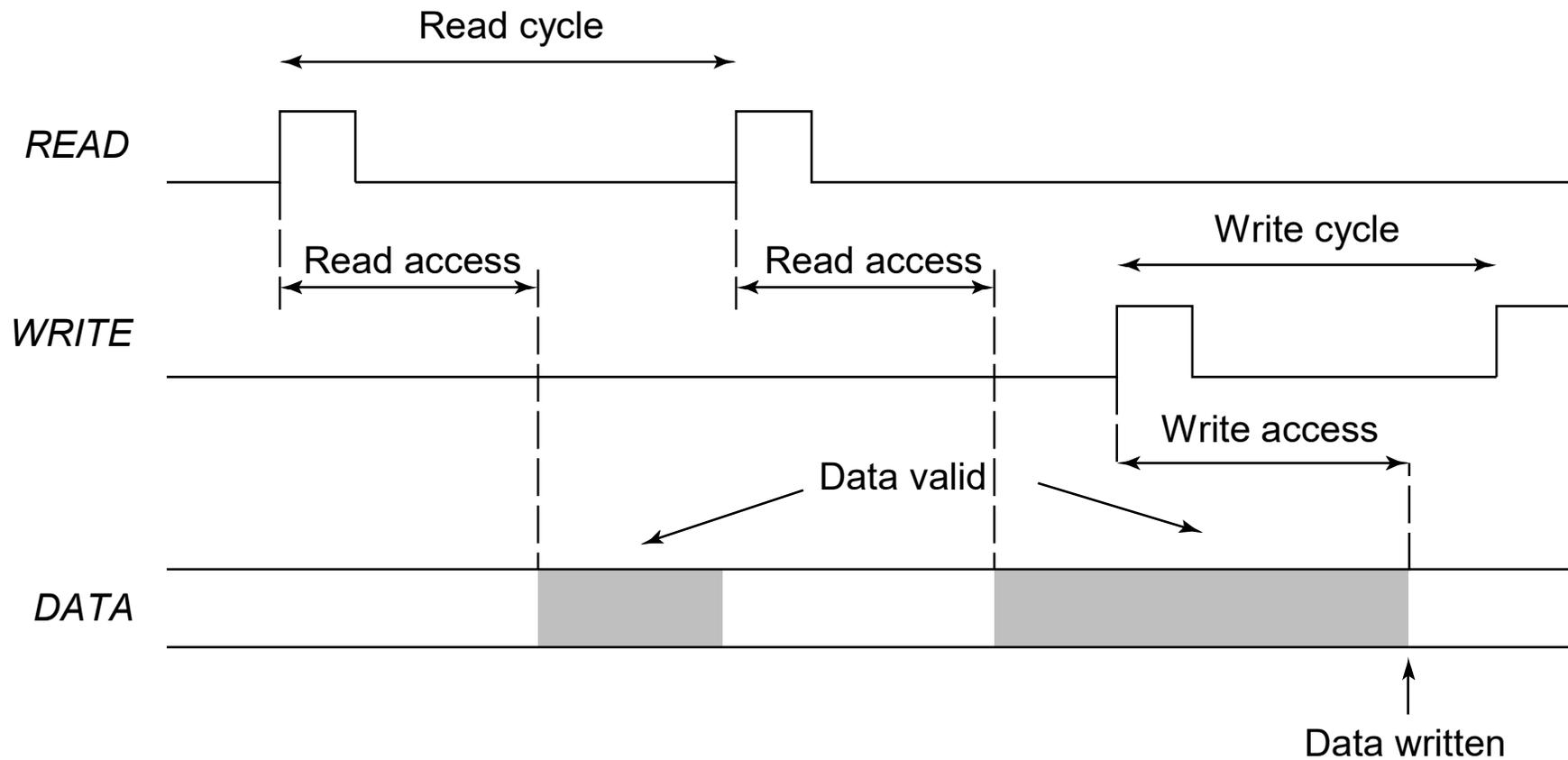


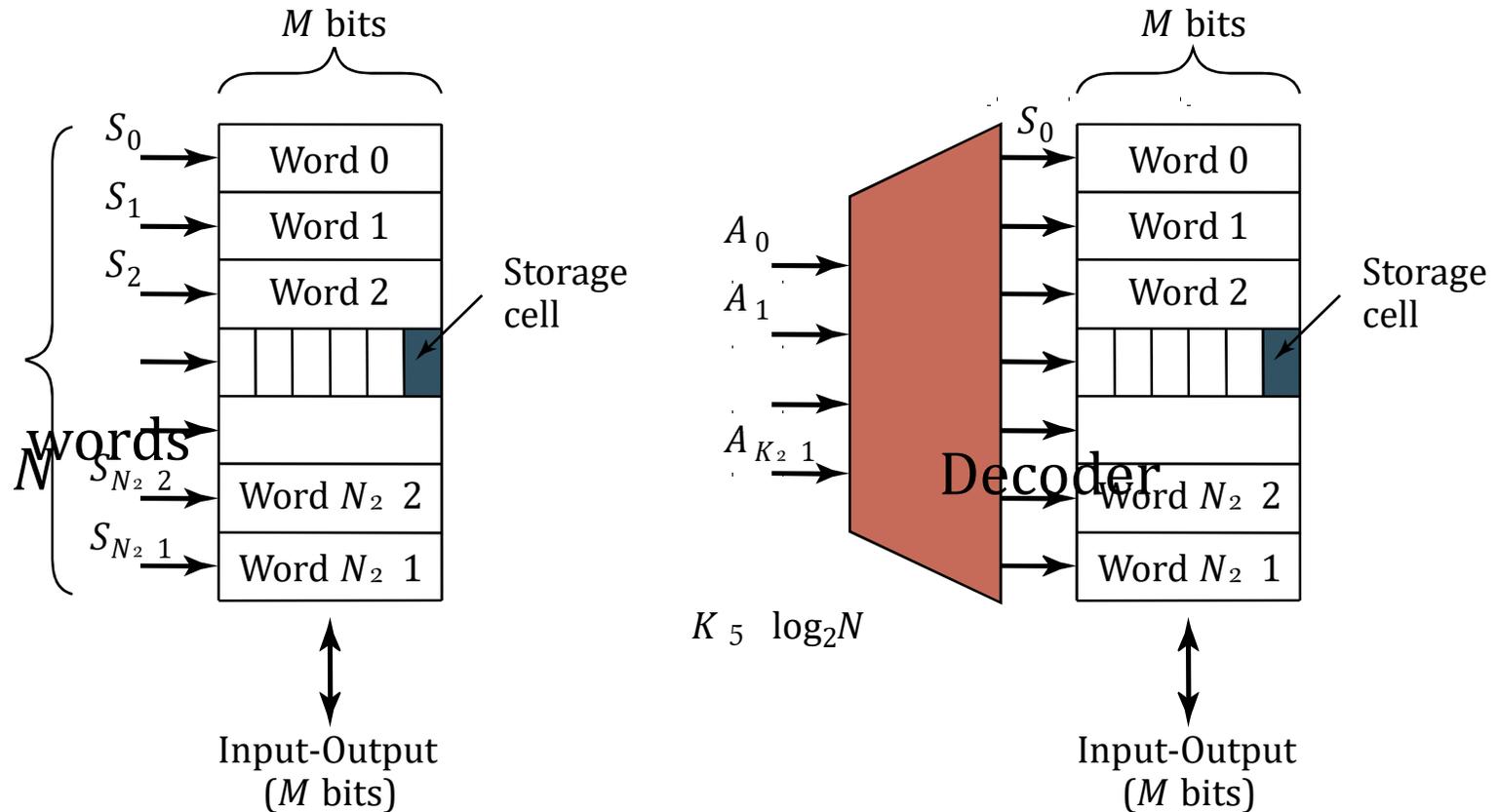
Semiconductor Memory Classification

Read-Write Memory		Non-Volatile Read-Write Memory	Read-Only Memory
Random Access	Non-Random Access	EPROM E ² PROM FLASH	Mask-Programmed Programmable (PROM)
SRAM DRAM	FIFO LIFO Shift Register CAM		

Memory Timing: Definitions



Memory Architecture: Decoders

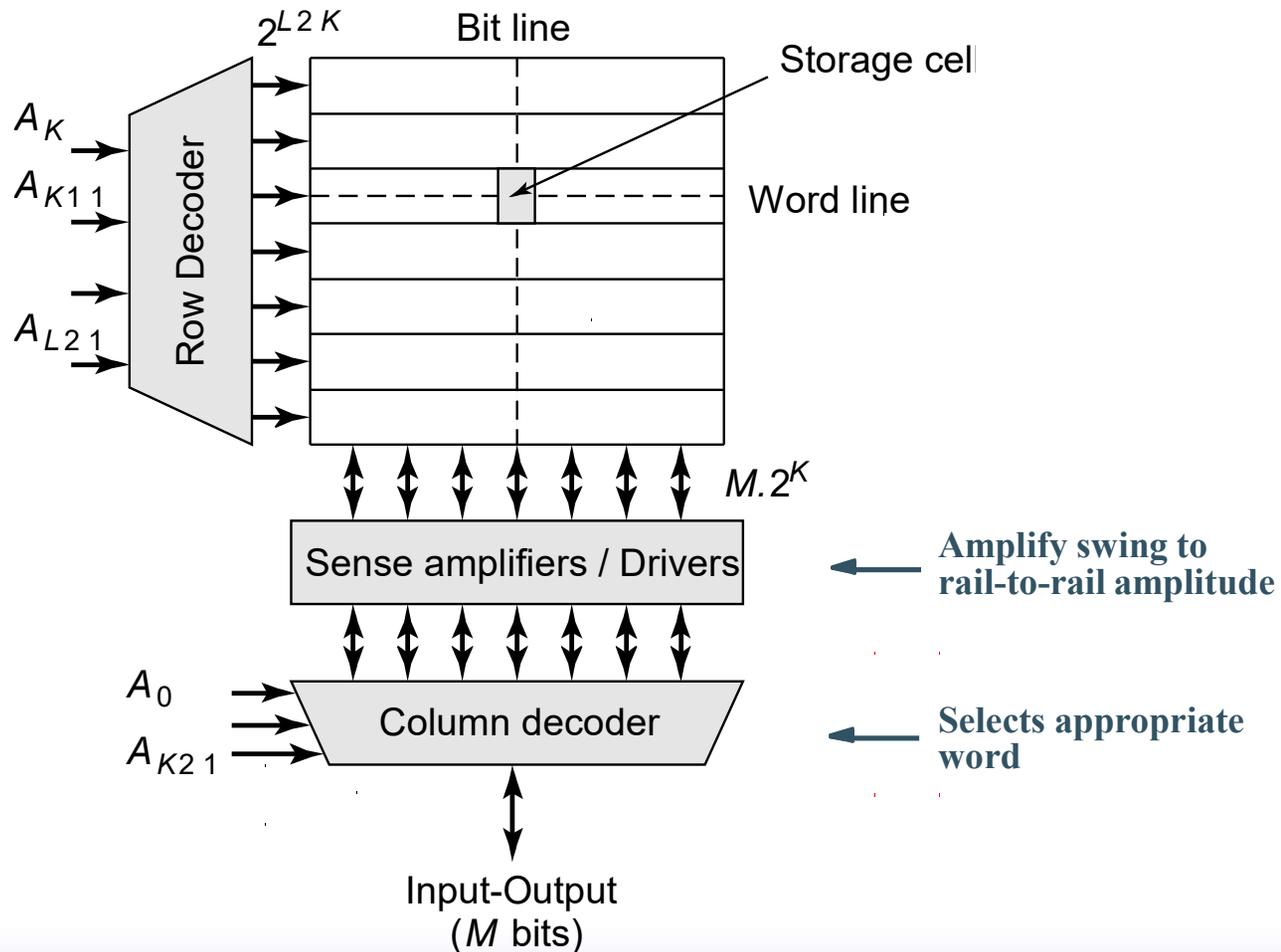


Intuitive architecture for $N \times M$ memory
 Too many select signals:
 N words == N select signals

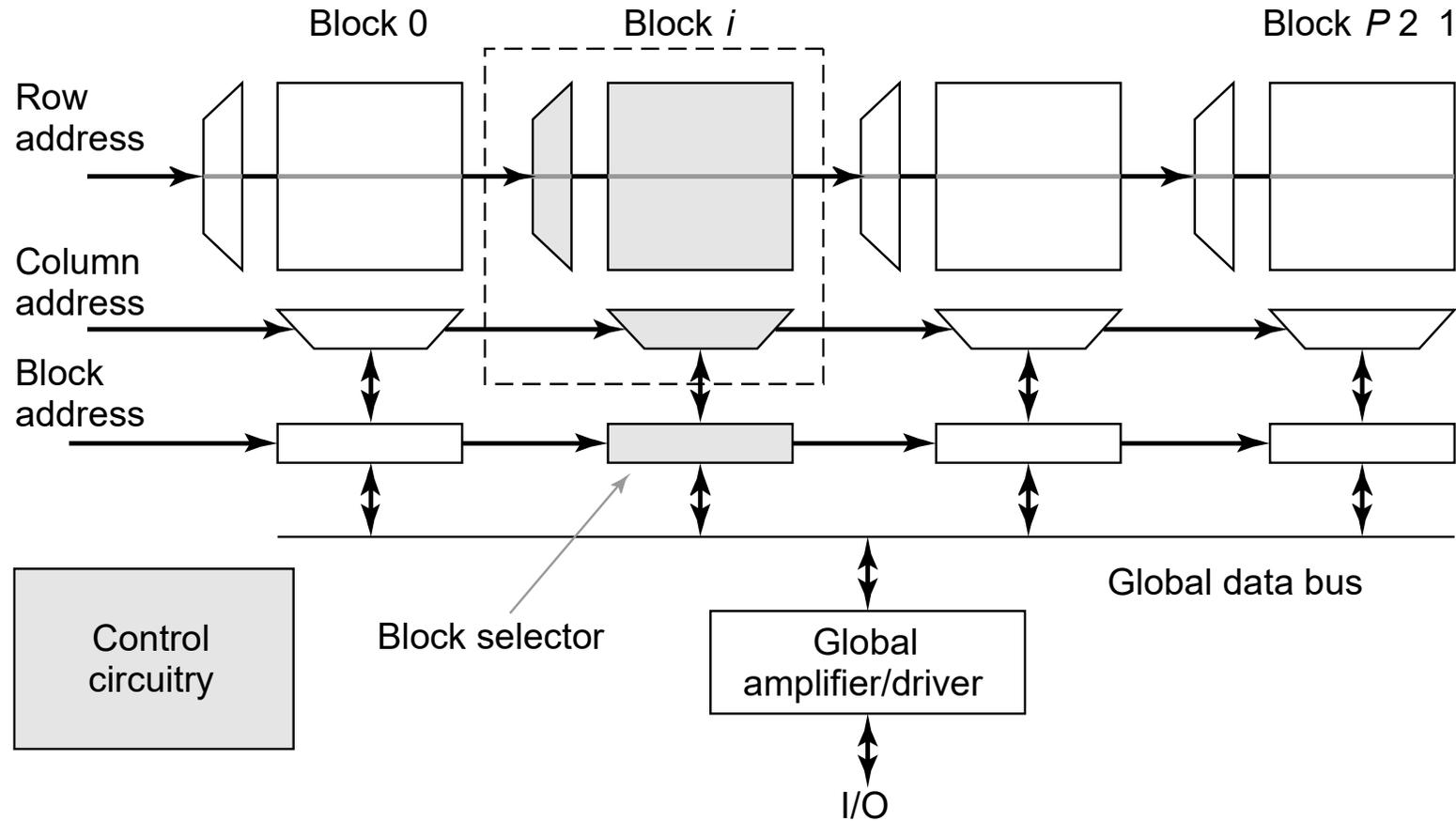
Decoder reduces the number of select signals
 $K = \log_2 N$

Array-Structured Memory Architecture

Problem: ASPECT RATIO or HEIGHT \gg WIDTH



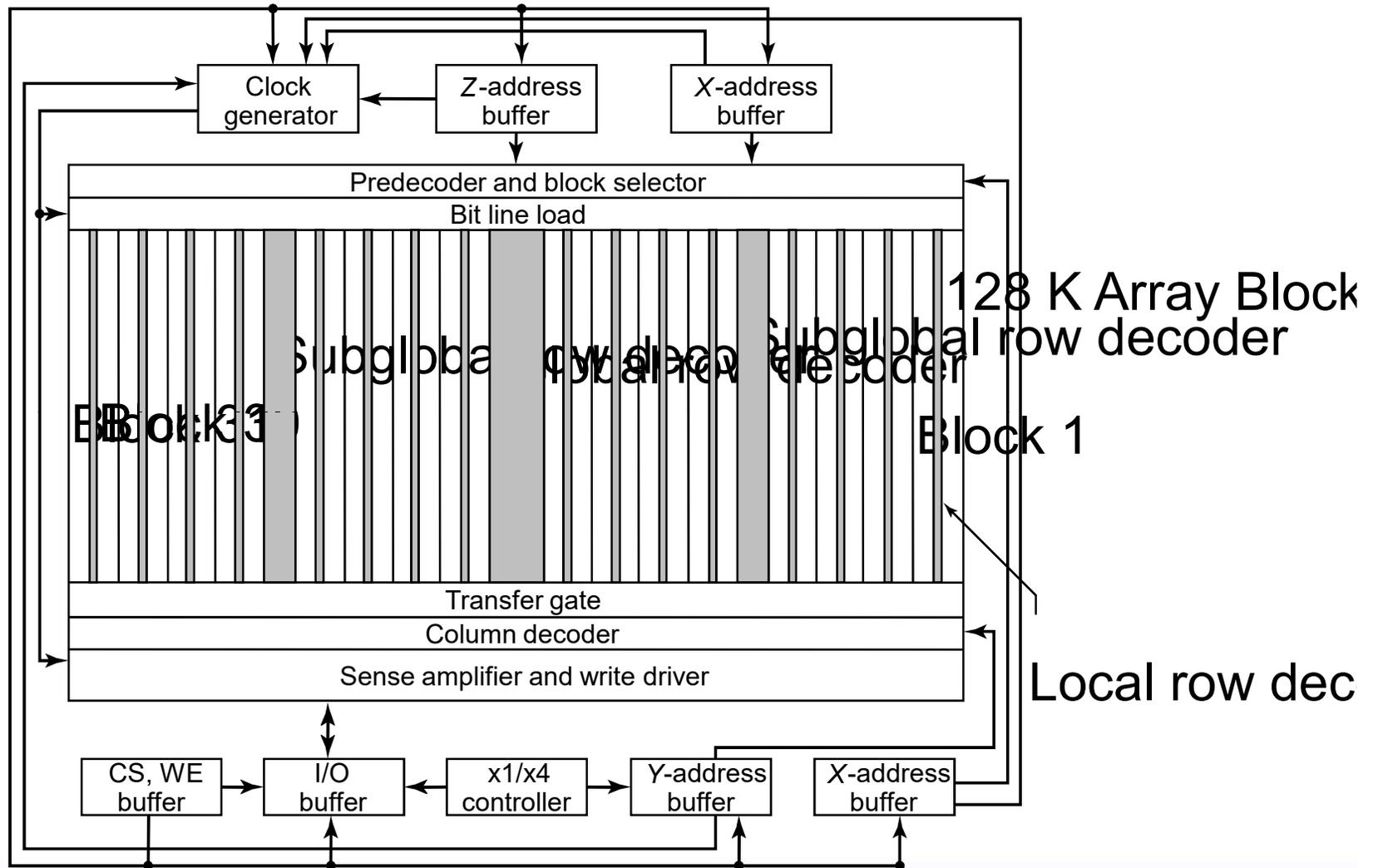
Hierarchical Memory Architecture



Advantages:

1. Shorter wires within blocks
2. Block address activates only 1 block => power savings

Block Diagram of 4 Mbit SRAM



Contents-Addressable Memory

