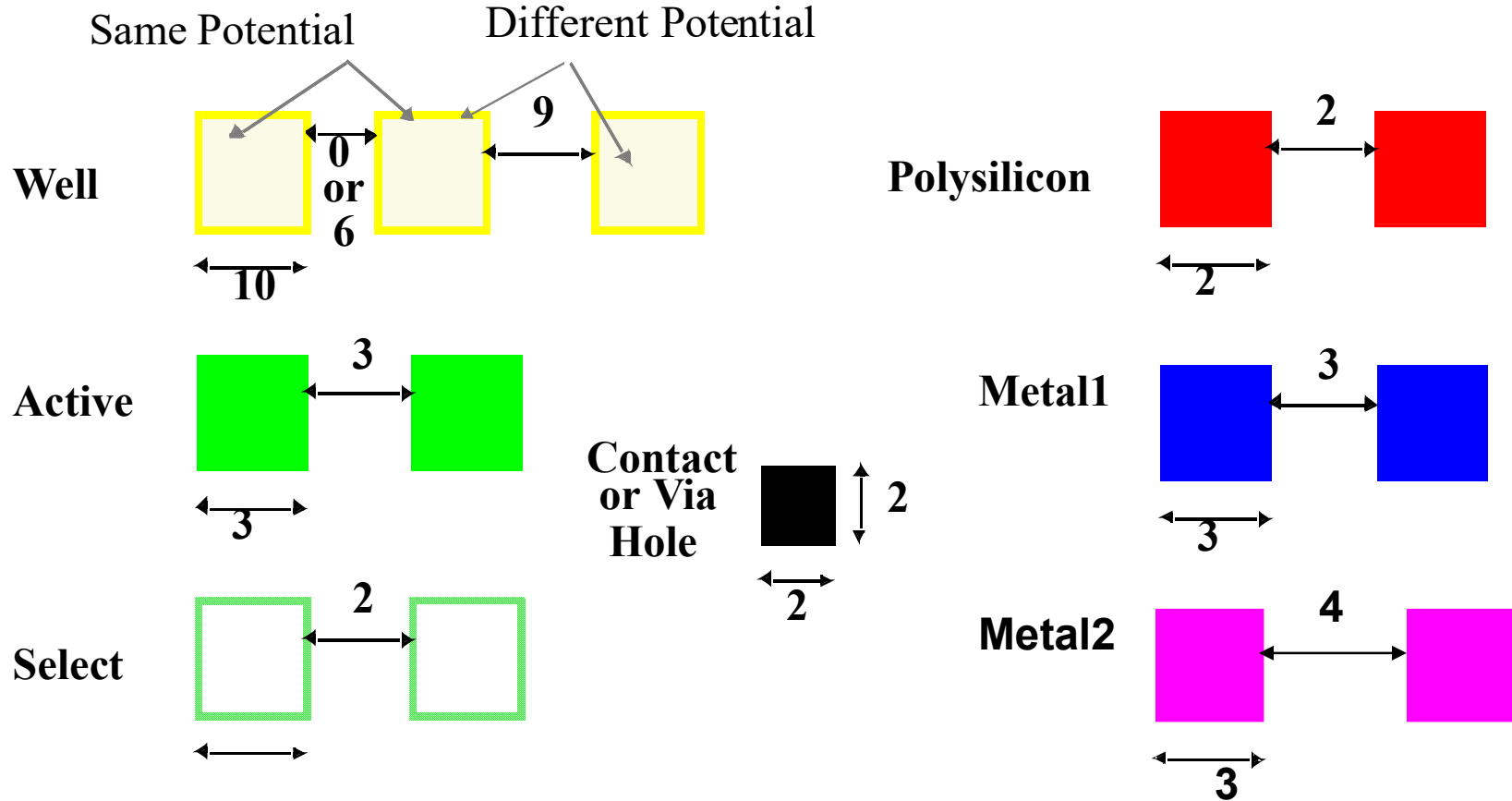
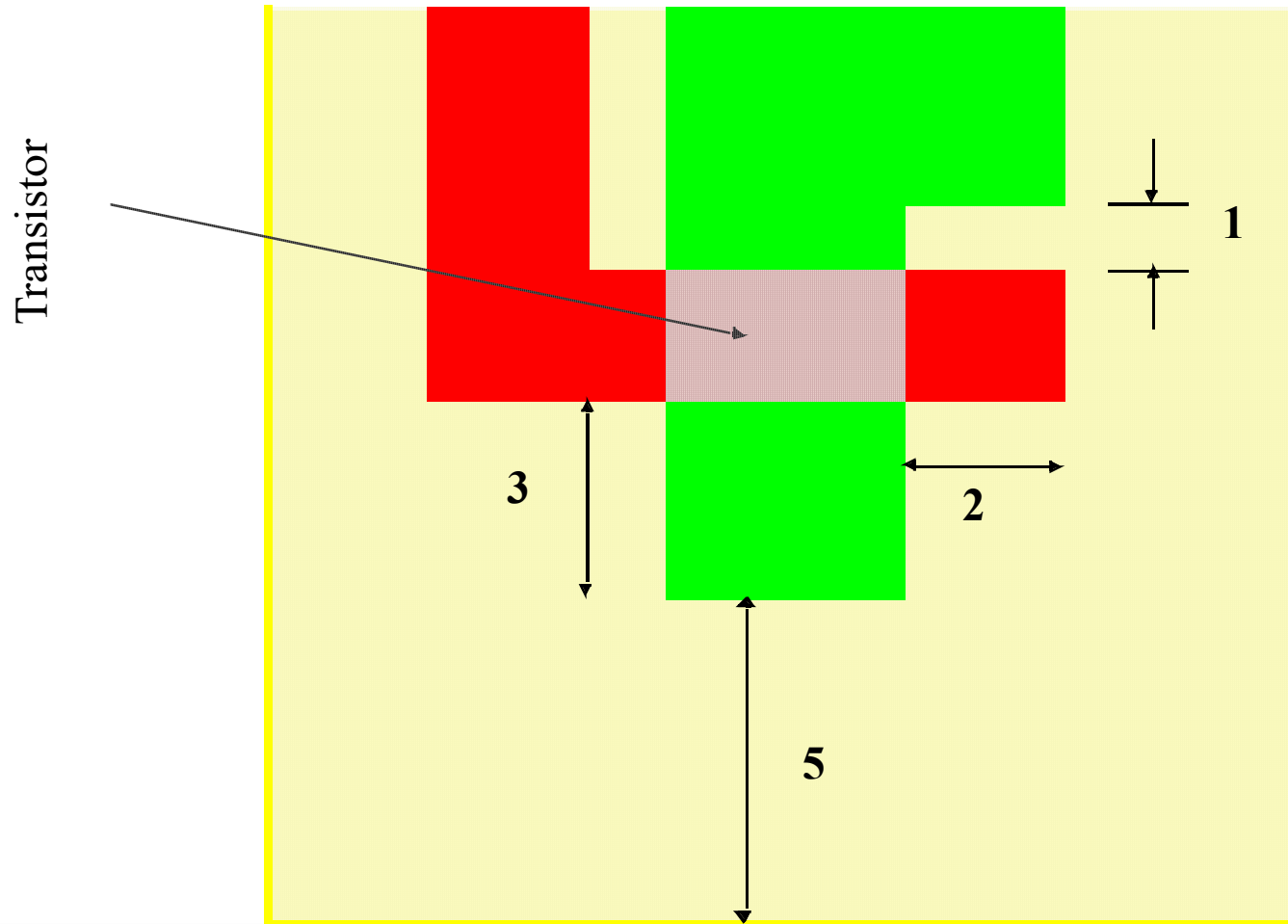


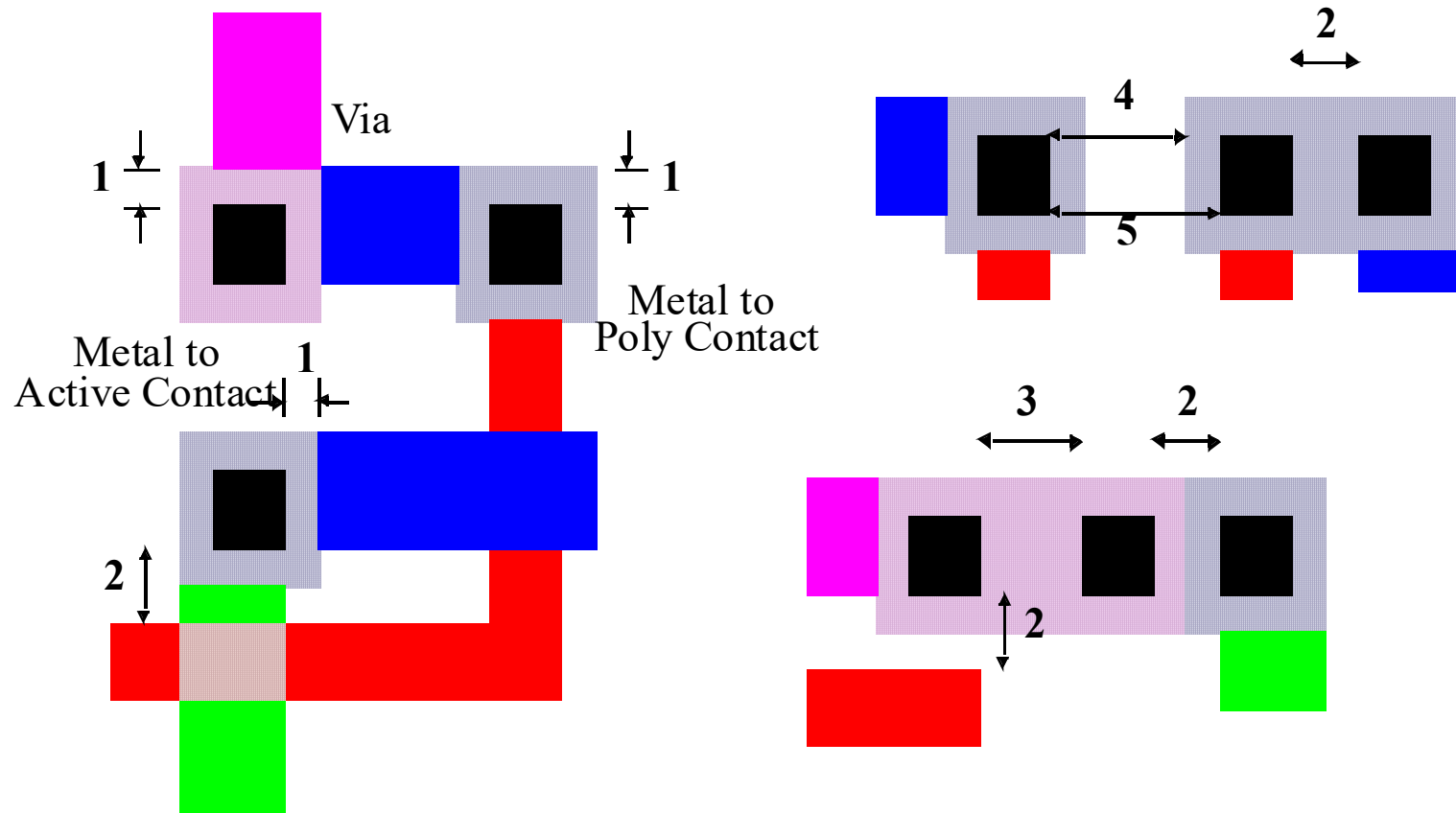
Intra-Layer Design Rules



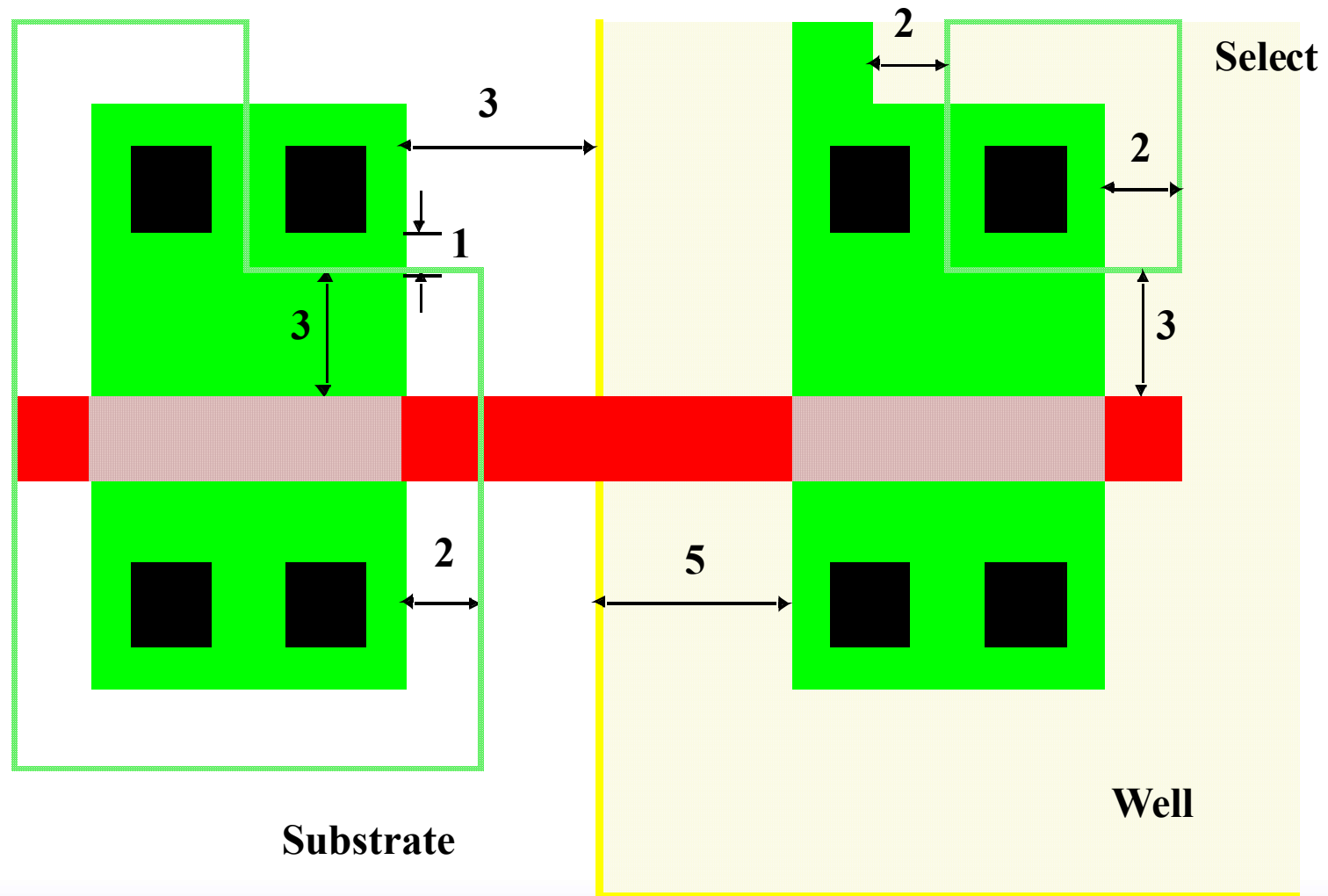
Transistor Layout



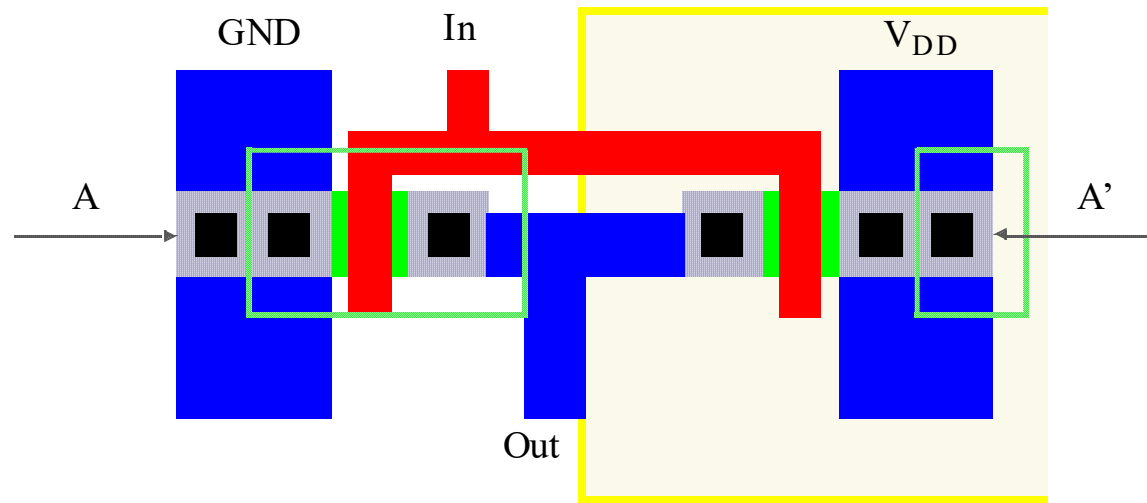
Vias and Contacts



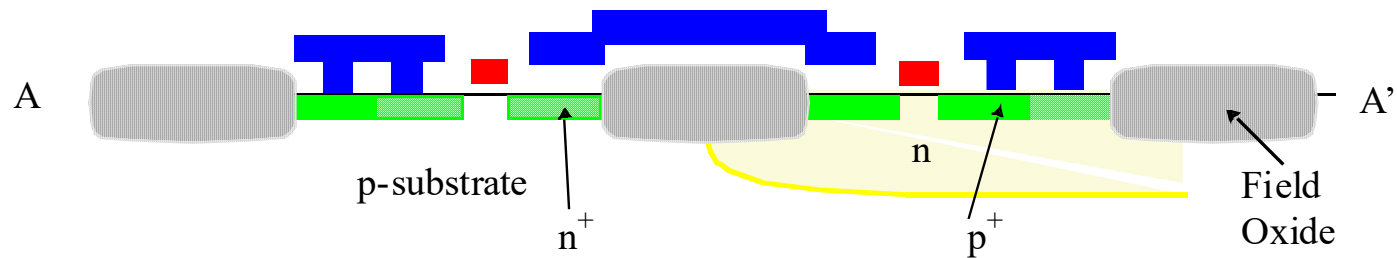
Select Layer



CMOS Inverter Layout

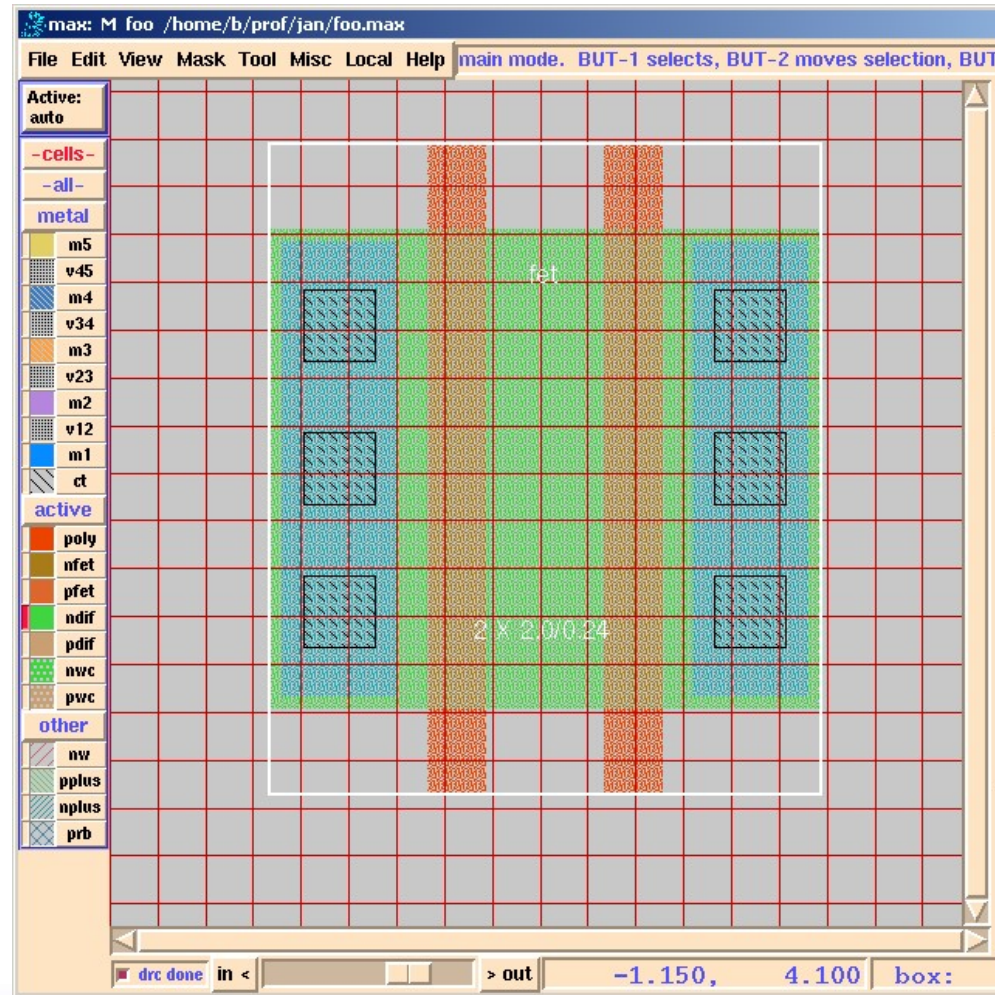


(a) Layout

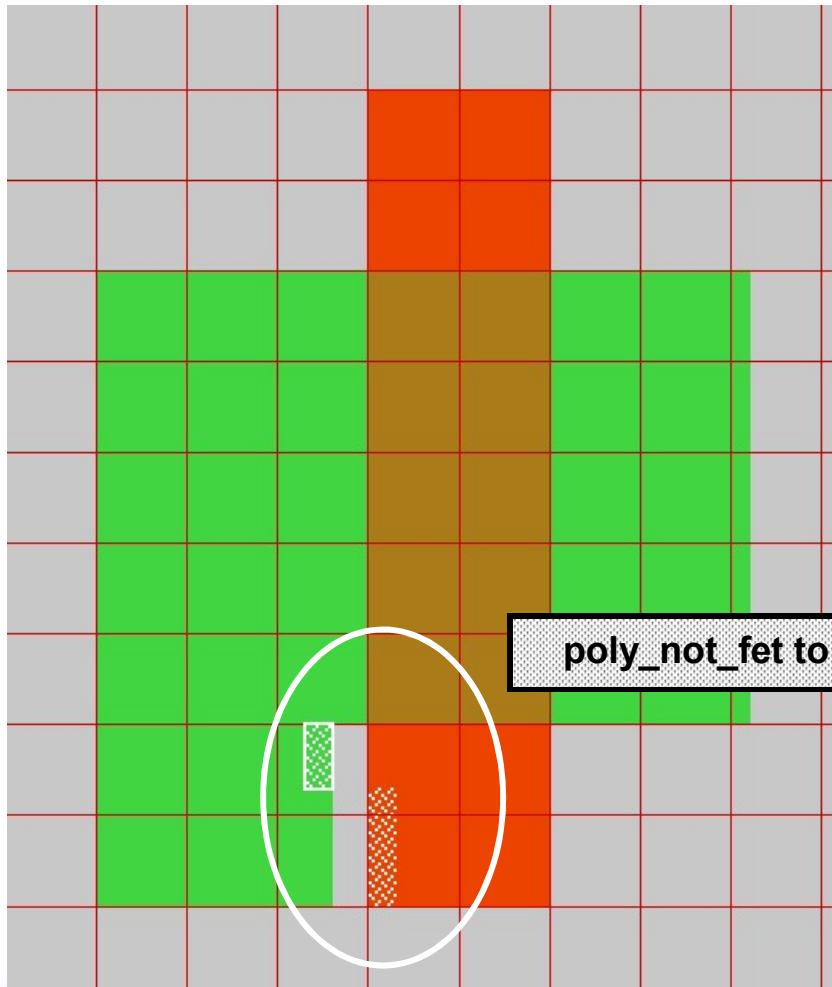


(b) Cross-Section along A-A'

Layout Editor

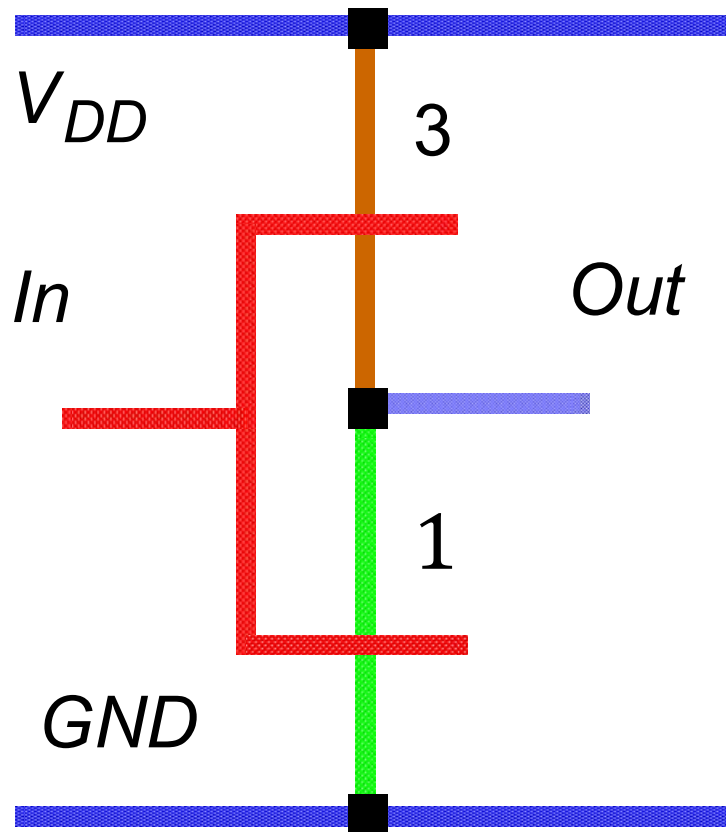


Design Rule Checker



poly_not_fet to all_diff minimum spacing = 0.14 um.

Sticks Diagram



Stick diagram of inverter

- Dimensionless layout entities
- Only topology is important
- Final layout generated by “compaction” program