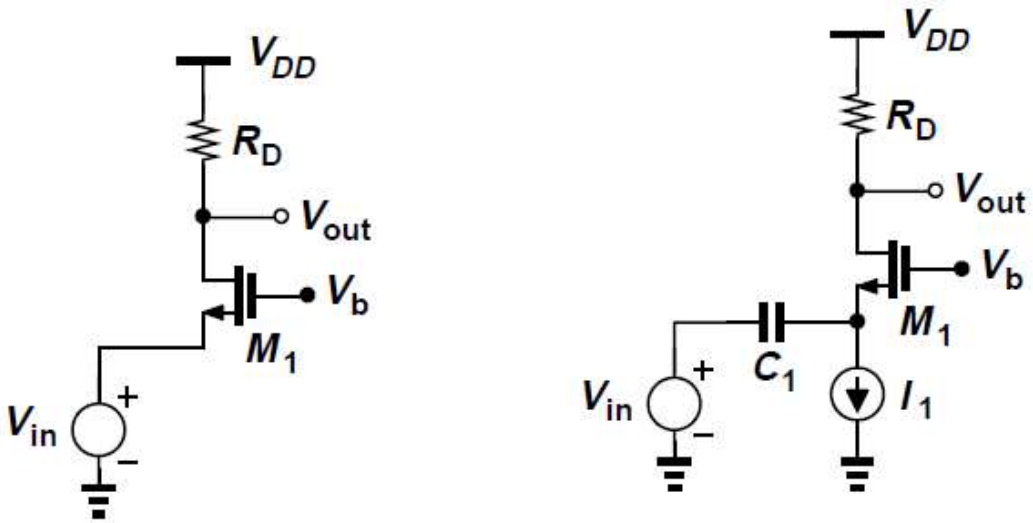
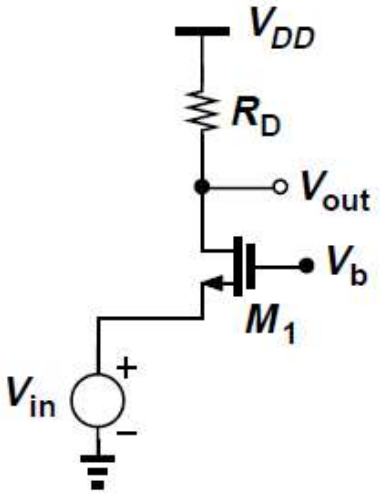
Common-Gate Stage

- A common-gate (CG) stage senses the input at the source and produces the output at the drain
- Gate is biased to establish proper operating conditions



- Bias current of M_1 flows through the input signal source
- Alternatively, M_1 can be biased by a constant current source, with the signal capacitively coupled to the circuit

Common-Gate Stage: Large-signal behavior



- Assume V_{in} decreases from a large positive value and that $\lambda=0$
- For $V_{in} \geq V_b - V_{TH}$, M_1 is off and $V_{out} = V_{DD}$
- For lower values of V_{in}, if M_1 is in saturation

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_b - V_{in} - V_{TH})^2$$

- As V_{in} decreases further, so does V_{out} driving M_1 into the triode region if

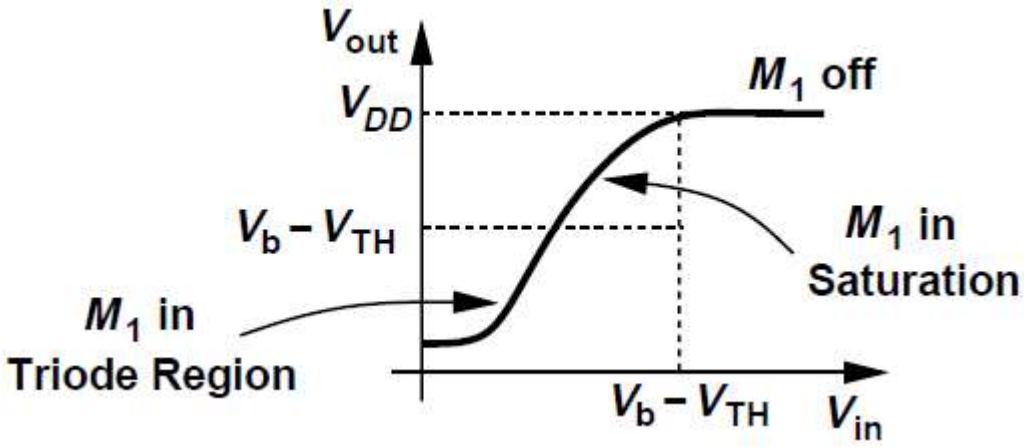
$$V_{DD} - \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_b - V_{in} - V_{TH})^2 R_D = V_b - V_{TH}$$

- In the region where M_1 is saturated, we can express the output voltage as

$$V_{out} = V_{DD} - \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_b - V_{in} - V_{TH})^2 R_D$$

Common-Gate Stage

Input-output characteristic



- For M_1 in saturation, $V_{out} = V_{DD} - \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_b - V_{in} - V_{TH})^2 R_D$

- Small-signal gain can thus be obtained

$$\frac{\partial V_{out}}{\partial V_{in}} = -\mu_n C_{ox}\frac{W}{L}(V_b - V_{in} - V_{TH})\left(-1 - \frac{\partial V_{TH}}{\partial V_{in}}\right) R_D$$

- Since $\partial V_{TH}/\partial V_{in} = \partial V_{TH}/\partial V_{SB} = \eta$, we have

$$\begin{aligned}\frac{\partial V_{out}}{\partial V_{in}} &= \mu_n C_{ox}\frac{W}{L}R_D(V_b - V_{in} - V_{TH})(1+\eta) \\ &= g_m(1+\eta)R_D.\end{aligned}$$

Common-Gate Stage

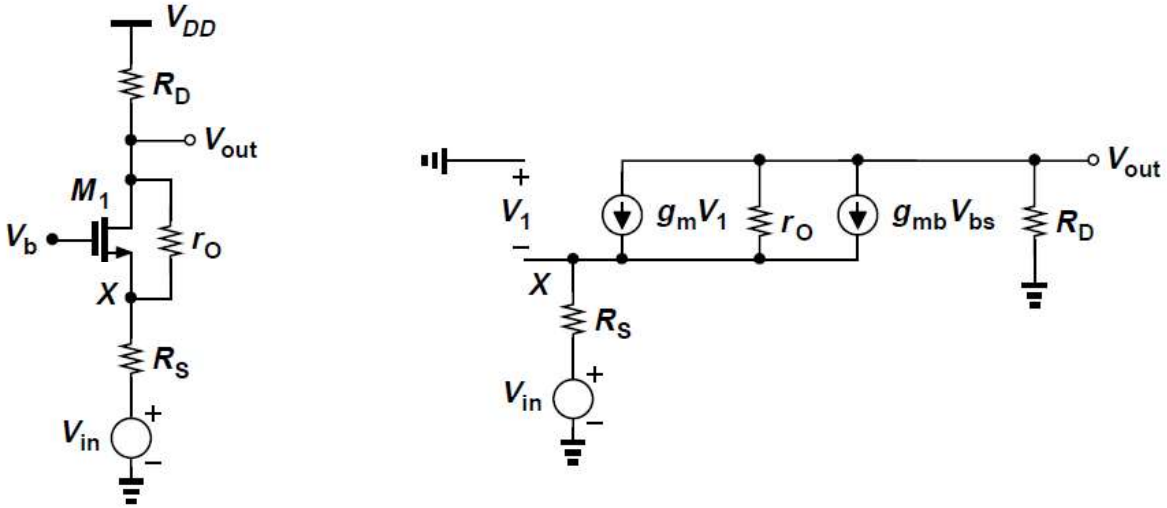
- Gain of the common-gate (CG) stage is positive

$$\begin{aligned}\frac{\partial V_{out}}{\partial V_{in}} &= \mu_n C_{ox}\frac{W}{L}R_D(V_b - V_{in} - V_{TH})(1+\eta)\\ &= g_m(1+\eta)R_D.\end{aligned}$$

- Body effect increases the effective transconductance of the stage
- For a given bias current and supply voltage (i.e., a given power budget), voltage gain of the CG stage can be maximized by
  - Increasing gm by widening the input device, eventually reaching subthreshold operation [$g_m = I_D/\zeta V_T$]
  - Increasing R_D and inevitably, the dc drop across it
- The minimum allowable value of V_{out} is $V_{GS}-V_{TH}+V_{I1}$, where V_{I1} denotes the minimum voltage required by I_1

Common-Gate Stage

- **Consider output impedance of transistor and impedance of the signal source**



- **In small-signal equivalent circuit, since current flowing R_S is $-V_{out}/R_D$,**

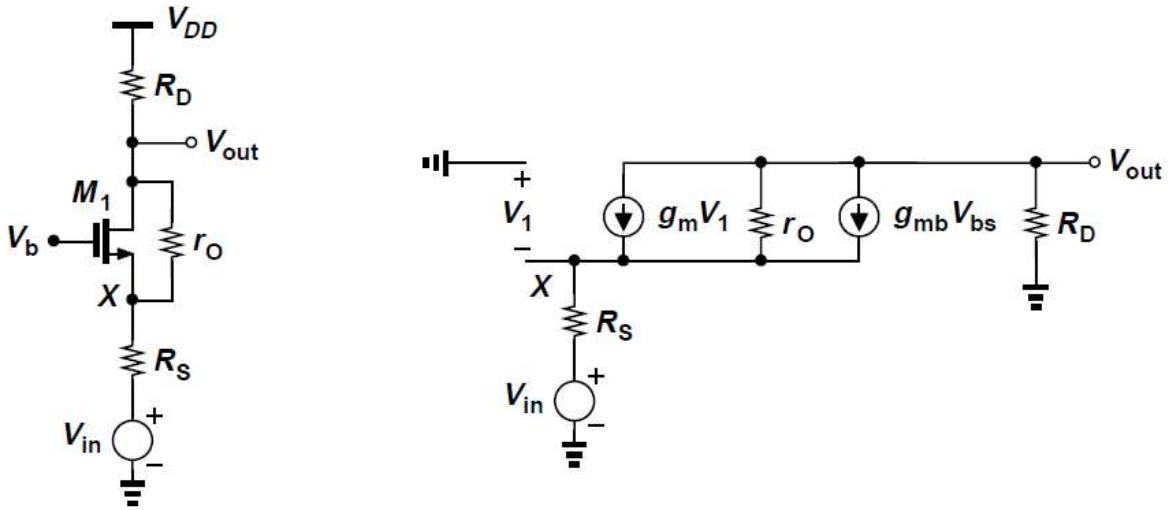
$$V_1 - \frac{V_{out}}{R_D} R_S + V_{in} = 0 \qquad \textbf{(1)}$$

$$-V_{out}/R_D - g_m V_1 - g_{mb} V_1$$

- **Moreove**

$$r_O \left(\frac{-V_{out}}{R_D} - g_m V_1 - g_{mb} V_1 \right) - \frac{V_{out}}{R_D} R_S + V_{in} = V_{out} \qquad \textbf{(2)}$$

Common-Gate Stage



- **Substituting V_1 from (1) in (2),**

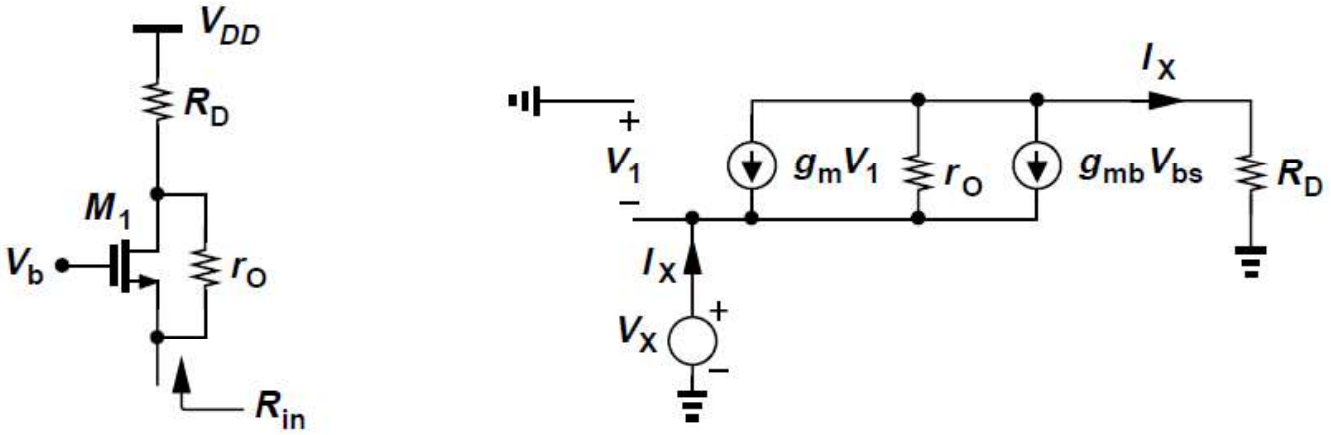
$$r_O\left[\frac{-V_{out}}{R_D}-(g_m+g_{mb})\left(V_{out}\frac{R_S}{R_D}-V_{in}\right)\right]-\frac{V_{out}R_S}{R_D}+V_{in}=V_{out}$$

- **Therefore,**

$$\frac{V_{out}}{V_{in}}=\frac{(g_m+g_{mb})r_O+1}{r_O+(g_m+g_{mb})r_O R_S+R_S+R_D}R_D$$

- **The voltage gain expression is similar to that of a degenerated CS stage**

Common-Gate Stage: Input Impedance



- From the small-signal equivalent circuit for finding input impedance, we have

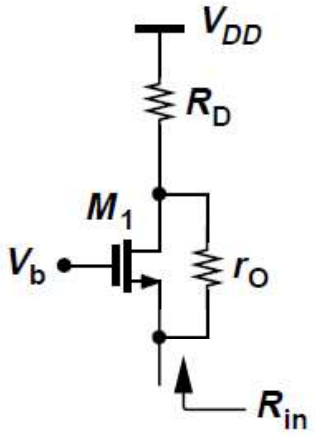
$$V_1 = -V_X$$

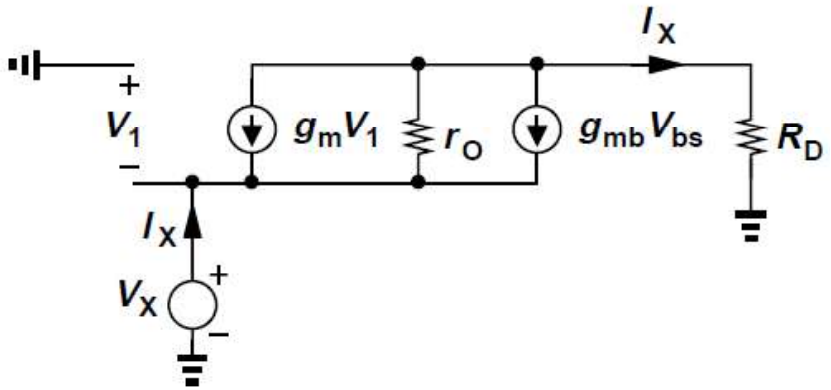
- The current through r_O is equal to $I_X + g_m V_1 + g_{mb} V_1 = I_X - (g_m + g_{mb}) V_X$

- Voltages across r_O and R_D can be added and equated to

$$R_D I_X + r_O [I_X - (g_m + g_{mb}) V_X] = V_X$$

Common-Gate Stage: Input Impedance





- **Thus,**

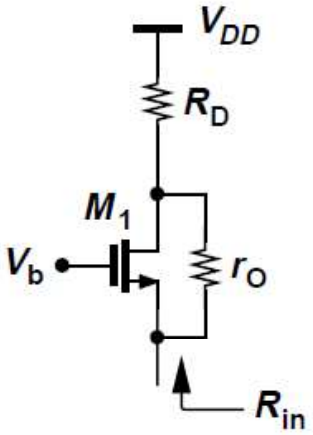
$$\frac{V_X}{I_X} = \frac{R_D + r_O}{1 + (g_m + g_{mb}) r_O}$$

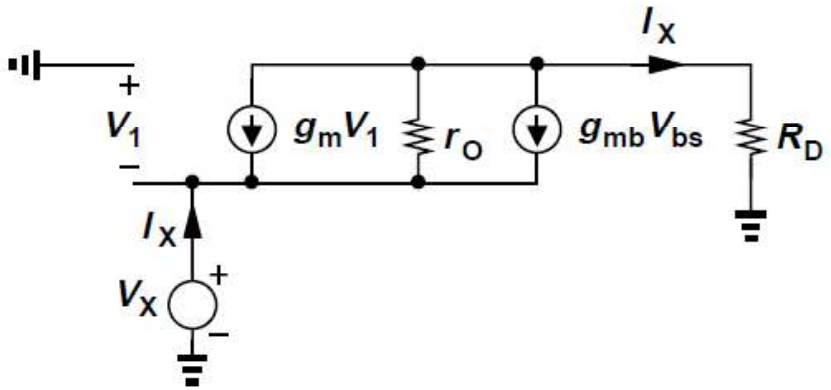
$$\approx \frac{R_D}{(g_m + g_{mb}) r_O} + \frac{1}{g_m + g_{mb}}$$

If $(g_m + g_{mb})r_O >> 1$

- **The drain impedance is divided by $(g_m + g_{mb})r_O$ when seen at the source**
  - **Important in short-channel devices because of their low intrinsic gain**

Common-Gate Stage: Input Impedance





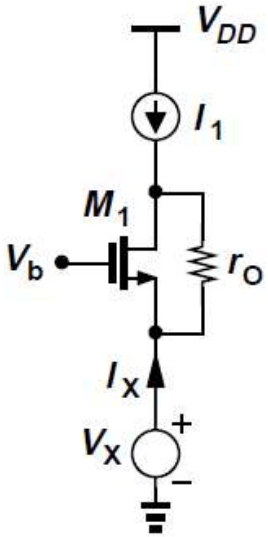
- **Suppose $R_D = 0$, then**

$$\frac{V_X}{I_X} = \frac{r_O}{1 + (g_m + g_{mb}) r_O}$$

$$= \frac{1}{\frac{1}{r_O} + g_m + g_{mb}},$$

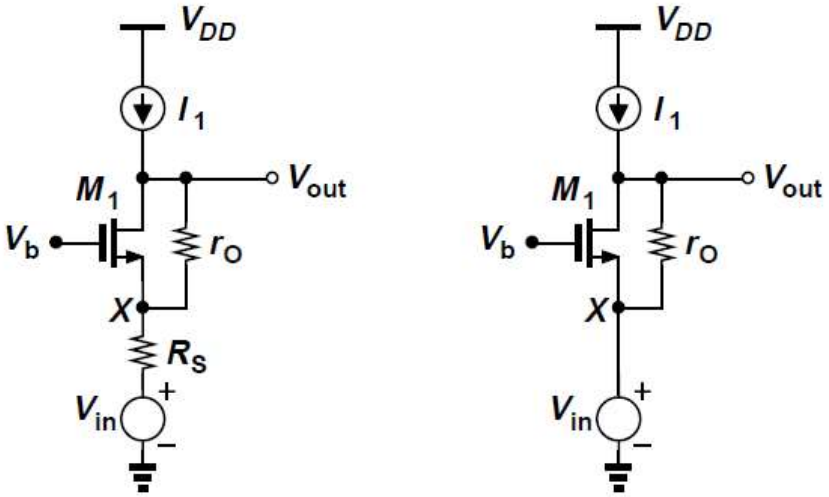
- **This is the impedance seen at the source of a source follower, a predictable result since with $R_D = 0$ the circuit configuration is the same as a source follower**

Common-Gate Stage: Input Impedance



- If R_D is replaced with an ideal current source, earlier result predicts that input impedance approaches infinity
- Total current through the transistor is fixed and is equal to I_1
- Therefore, a change in the source potential cannot change the device current, and hence $I_X = 0$
- The input impedance of a CG stage is relatively low *only* if the load impedance connected to the drain is small

Common-Gate Stage

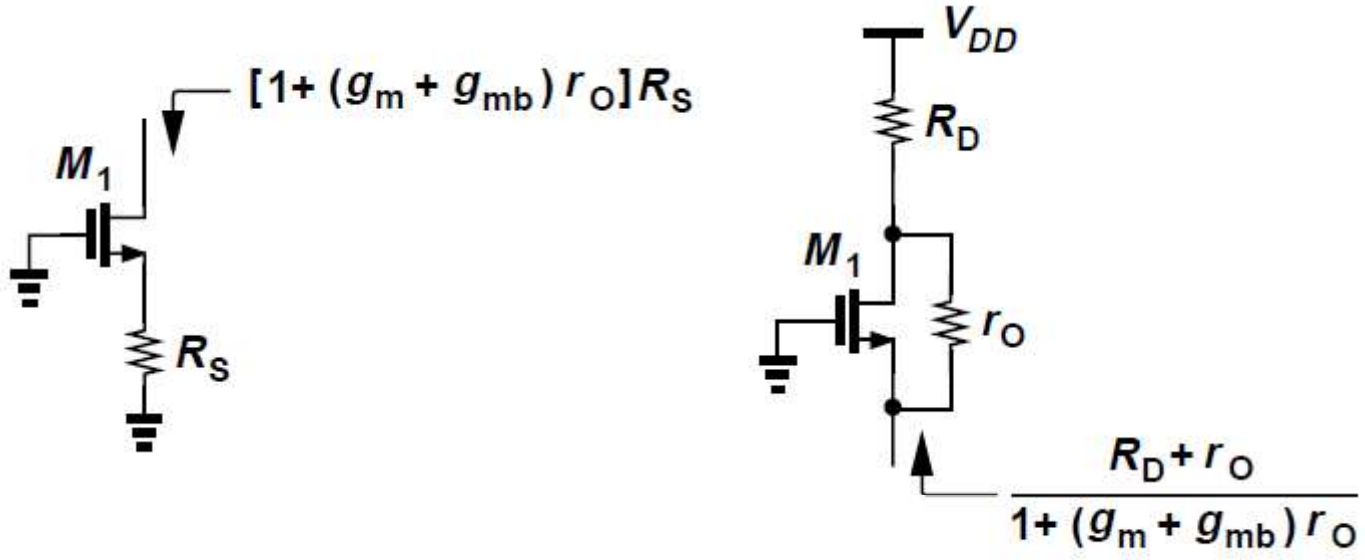


- **In a CG stage with a current source load, substituting $R_D=\infty$ in the voltage gain equation, we get**

$$A_v = (g_m + g_{mb})r_O + 1$$

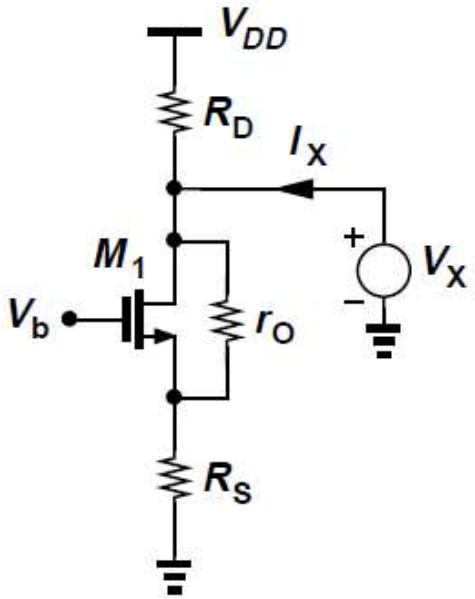
- **Gain does not depend on R_S**
- **From the foregoing discussion, if $R_D \to \infty$, so does the impedance seen at the source of M_1, and the small-signal voltage at node X becomes equal to V_{in}**

Common-Gate Stage



- **In a degenerated CS stage, we loosely say that a transistor transforms its source resistance *up***
- **In a CG stage, the transistor transforms its drain resistance *down***
- **The MOS transistor can thus be viewed as an resistance transformer**

Common-Gate Stage: Output Impedance



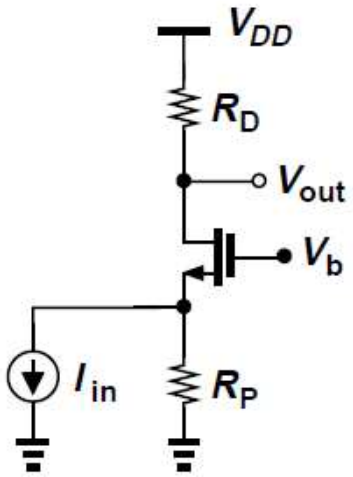
- From the above small-signal equivalent circuit, we can find output impedance as

$$R_{out} = \{[1 + (g_m + g_{mb})r_O]R_S + r_O\} \| R_D$$

- Result is similar to that obtained for a degenerated CS stage

Common-Gate Stage

- Input signal of a common-gate stage may be a current rather than a voltage as shown below



- Input current source exhibits output impedance of R_P
- To find the "gain" V_{out}/I_{in}, replace I_{in} and R_P with a Thevenin equivalent and use derived result to write

$$\frac{V_{out}}{I_{in}} = \frac{(g_m + g_{mb})r_O + 1}{r_O + (g_m + g_{mb})r_O R_P + R_P + R_D} R_D R_P$$

$$R_{out} = \{[1 + (g_m + g_{mb})r_O]R_P + r_O\} \| R_D$$

- Output impedance is simply given by