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## Drain Induced Barrier Lowering (DIBL)

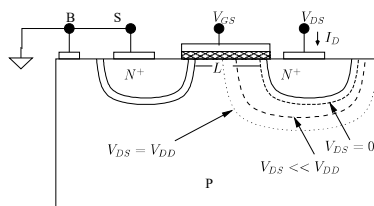


Figure: NMOS Transistor DIBL

- ▶ Drain controls amount of depletion in the channel
- ▶ Easier for the gate to invert with higher  $V_{DS}$
- ▶ Gate effectively has lesser control

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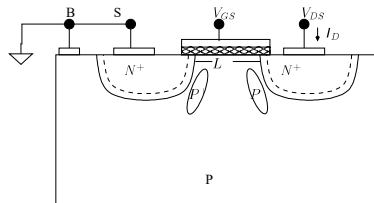
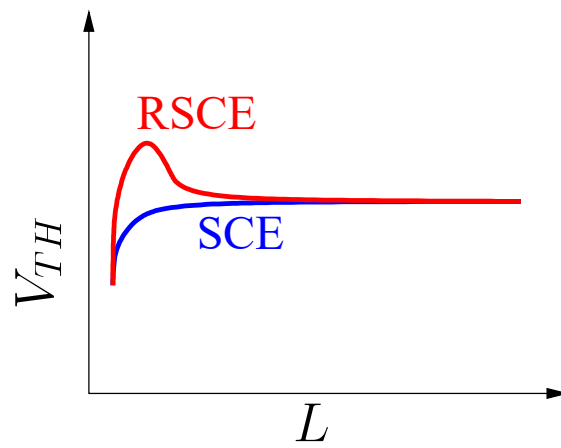


Figure: NMOS Transistor with Halo Implant

- ▶  $P^+$  halo added near diffusion
- ▶ Depletion layer now goes deeper into the diffusion rather than channel
- ▶ Gate has better control now
- ▶  $DIBL = \frac{V_{TH}(V_{DS}=V_{DD}^H) - V_{TH}(V_{DS}=V_{DD}^L)}{V_{DD}^H - V_{DD}^L}$

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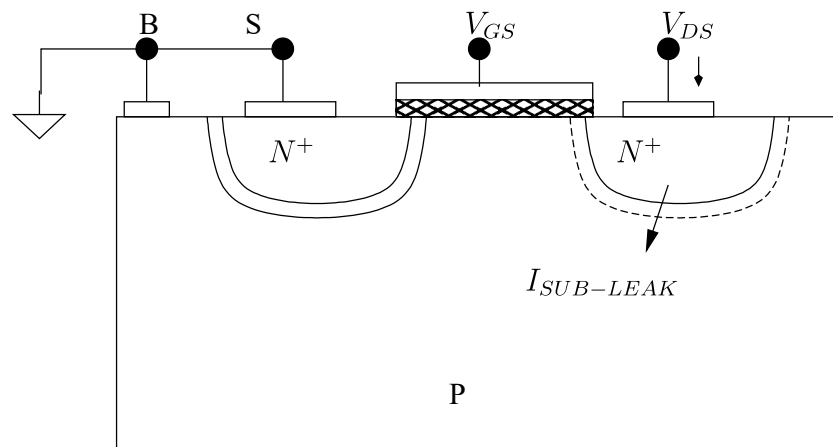
## Reverse Short Channel Effect



Halo implant makes it harder to invert the channel

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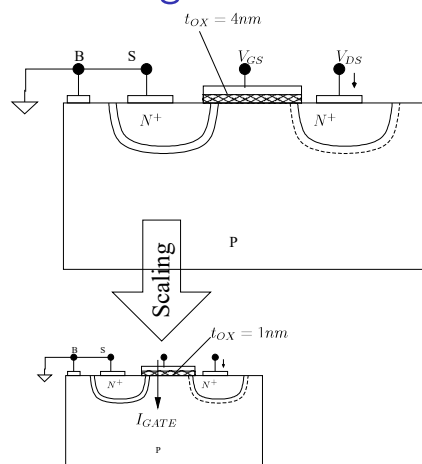
## Substrate Leakage



Reverse biased  $P - N^+$  junction leakage

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## Gate Leakage



- ▶ Quantum mechanical tunneling across the gate oxide
- ▶ Use of  $HfO_2$  - HiK dielectric since 45nm technology