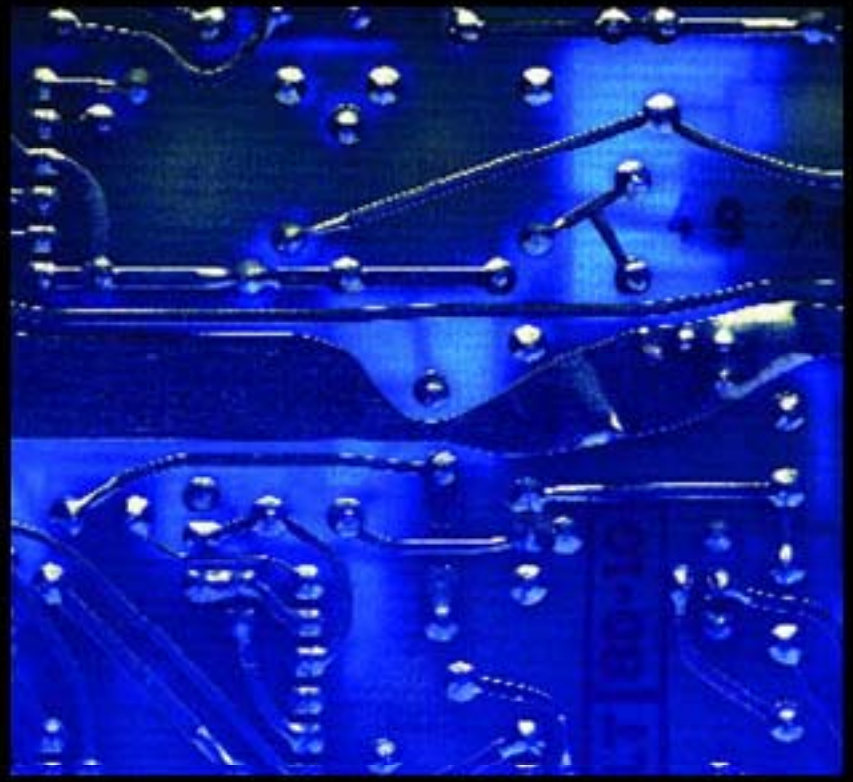
ELECTRONIC DEVICES AND CIRCUIT THEORY

TENTH EDITION



BOYLESTAD

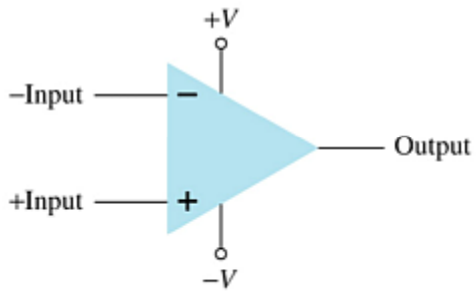
PEARSON

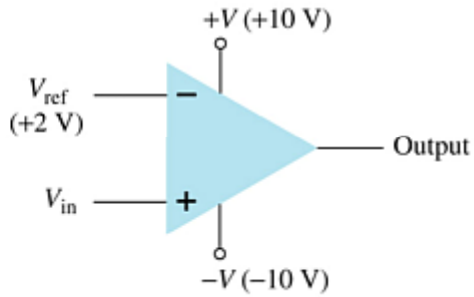
Chapter 13
Linear-Digital ICs

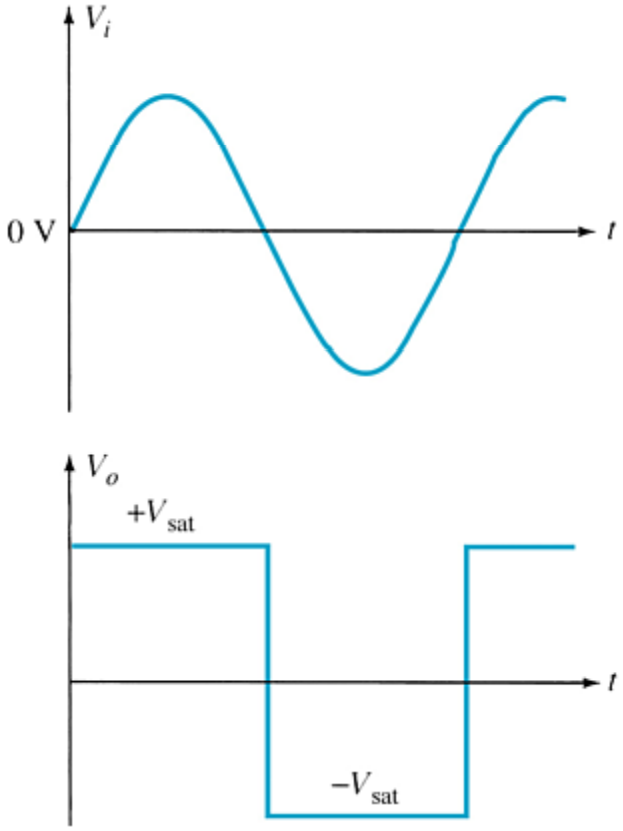
Linear Digital ICs

Comparators
Digital/analog converters
Timers
Voltage-controlled oscillators
Phase-locked loop circuits
Interface circuits

Comparator Circuit







The operation is a basic comparison. The output swings between its maximum and minimum voltage, depending upon whether one input (V_{in}) is greater or less than the other (V_{ref}).

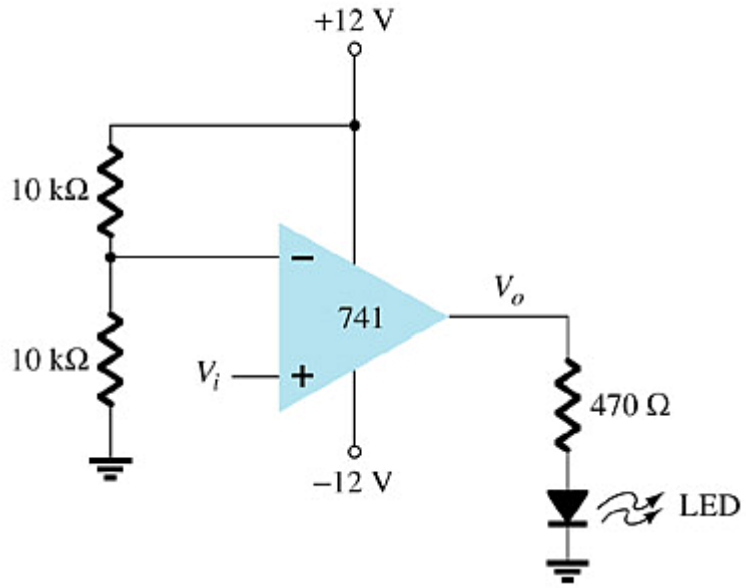
The output is always a square wave where:

- **The maximum high output voltage is $+V_{SAT}$.**
- **The minimum low output voltage is $-V_{SAT}$.**

Noninverting Op-Amp Comparator

For a noninverting op-amp comparator:

- **The output goes to $+V_{SAT}$ when input V_i is greater than the reference voltage.**
- **The output goes to $-V_{SAT}$ when input V_i is less than the reference voltage.**



Example:

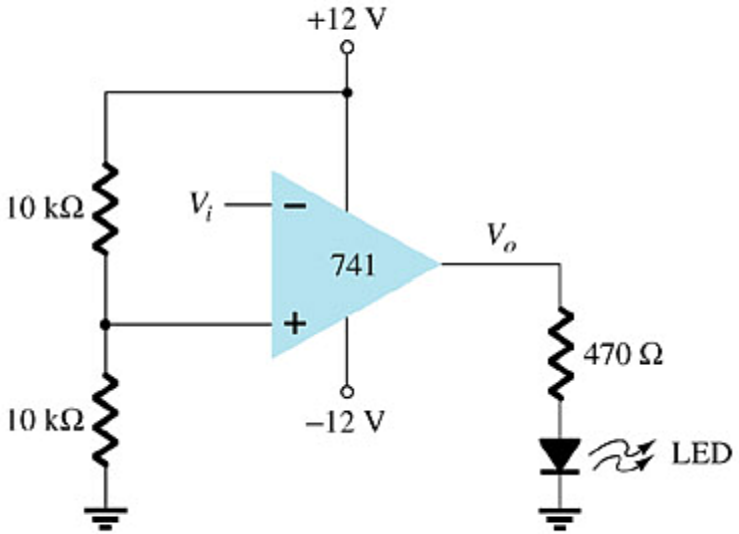
- **V_{ref} in this circuit is +6V (taken from the voltage divider)**
- **$+V_{SAT}$ = +V, or +12V**
- **$-V_{SAT}$ = –V or –12V**

When V_i is greater than +6V the output swings to +12V and the LED goes on.
When V_i is less than +6V the output is at –12V and the LED goes off.

Inverting Op-Amp Comparator

For an inverting op-amp comparator:

- **The output goes to $-V_{SAT}$ when input V_i is greater than the reference voltage.**
- **The output goes to $+V_{SAT}$ when input V_i is less than the reference voltage.**



Example:

- **V_{ref} in this circuit is +6V (taken from the voltage divider)**
- **$+V_{SAT} = +V$, or +12V**
- **$-V_{SAT} = -V$ or –12V**

When V_i is greater than +6V the output swings to –12V and the LED goes off.
When V_i is less than +6V the output is at +12V and the LED goes on.

Comparator ICs

Advantages:

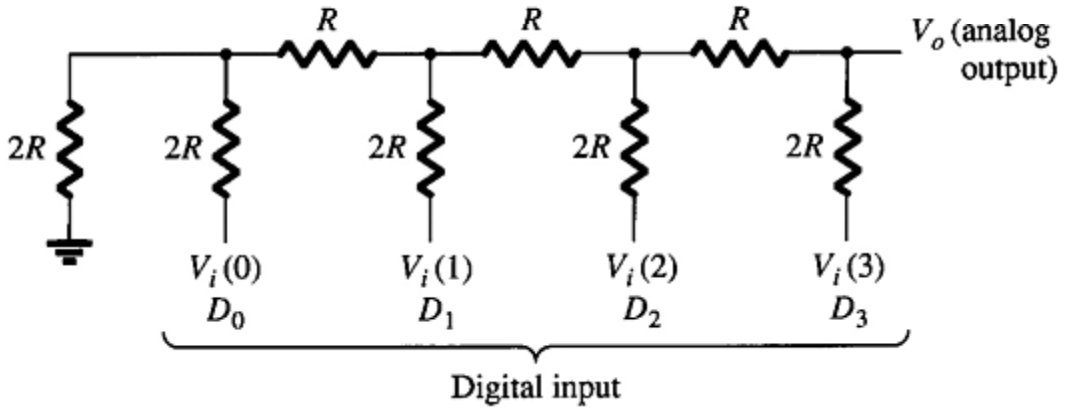
- **Faster switching**
- **Built-in noise immunity**
- **Outputs capable of directly driving loads**

Digital-Analog Converters

Types:

- **Digital-to-analog converters (ADCs)**
- **Analog-to-digital converters (DACs)**

Digital-to Analog Converter: Ladder Network Version



Output Voltage, V_o:

$$V_o = \frac{D_0 \times 2^0 + D_1 \times 2^1 + D_2 \times 2^2 + D_3 \times 2^3}{2^4} V_{ref}$$

Voltage Resolution:

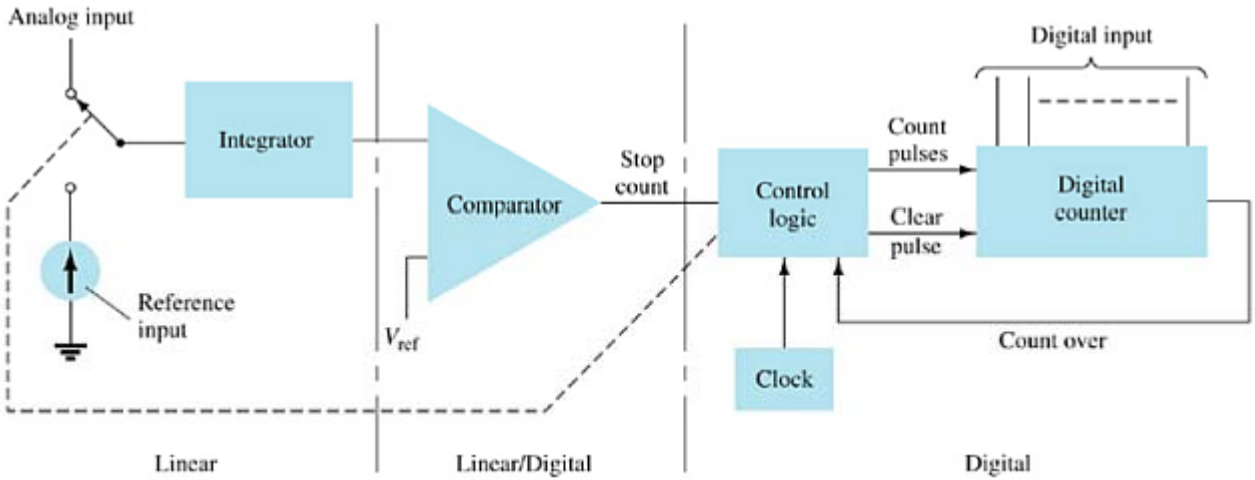
$$\frac{V_{ref}}{2^4}$$

Analog-to-Digital Converters

Types:

- **Dual Slope Conversion**
- **Ladder Network Conversion**

Analog-to-Digital Conversion
Dual Slope Conversion



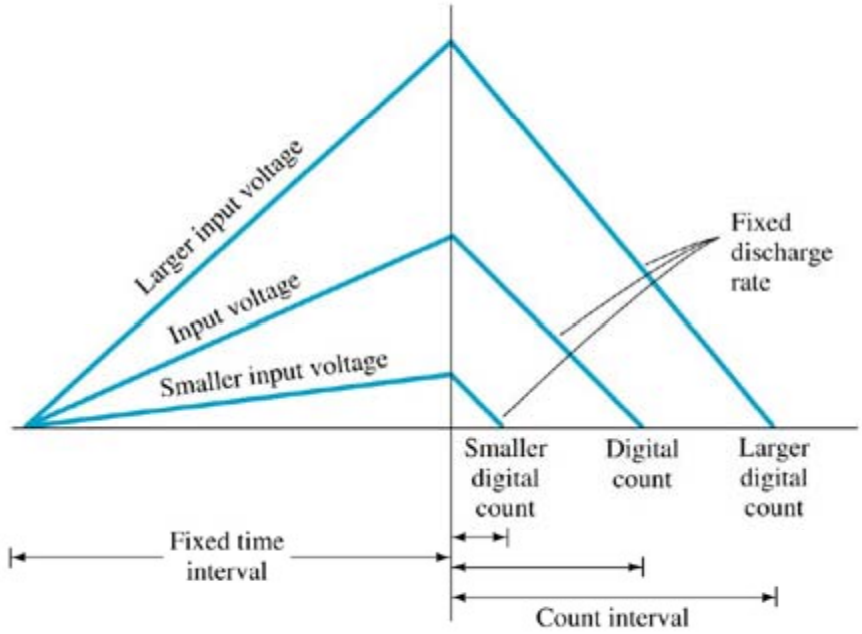
The analog input voltage is applied to an integrator or ramp-generator circuit.

The digital output is obtained from a digital counter that is operated during both positive and negative slope (ramp) intervals of the integrator.

Dual Slope Conversion

Rising Slope

For a fixed interval the analog voltage is applied to the integrator. The integrator output rises to some positive level. This positive voltage is applied to a comparator. At the end of the fixed interval, the counter is reset to 0. An electronic switch connects the integrator input to a fixed input or reference voltage.



Falling Slope

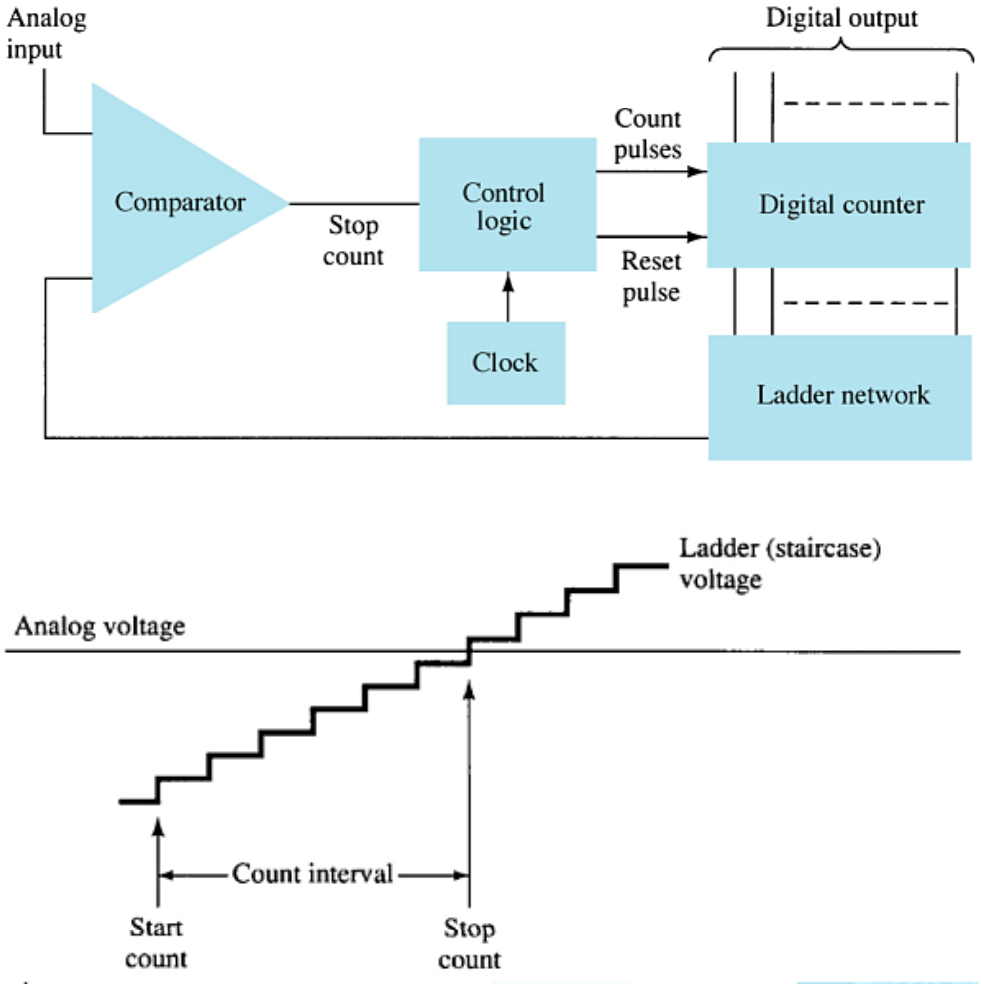
The integrator output decreases at a fixed rate. The counter advances during this time. When the integrator output (connected to the comparator input) falls below the reference level of the comparator, control logic stops the counter.The digital counter output is the digital conversion of the analog input.

Ladder Network Conversion

A digital counter advances from zero while a ladder network converts the digital count to a staircase analog voltage.

When the staircase voltage into the comparator equals the analog input voltage, the counter stops.

The last count is the digital conversion of the analog input.



Resolution of Analog-to-Digital Converters

The resolution depends on the amount of voltage per step (digital bit):

$$\frac{V_{ref}}{2^n}$$

where n is the number of digital bits

Example: A 12-bit ADC with a 10V reference level has the following resolution:

$$\frac{V_{ref}}{2^n} = \frac{10V}{2^{12}} = 2.4mV$$

Analog-to-Digital Conversion Time

The conversion time depends on the clock frequency of the counter.

$$T_{conv} = \frac{2^n}{f}$$

where

T_{conv} = conversion time (seconds)
n = number of binary bits
f = clock frequency for the counter

Example: A 12bit ADC with a 1MHz clock has a maximum conversion time.

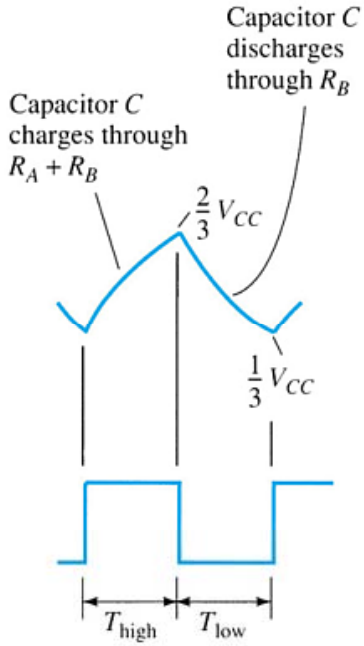
$$2^{12}\left(\frac{1}{1\text{MHz}}\right) = 4.1\text{ms}$$

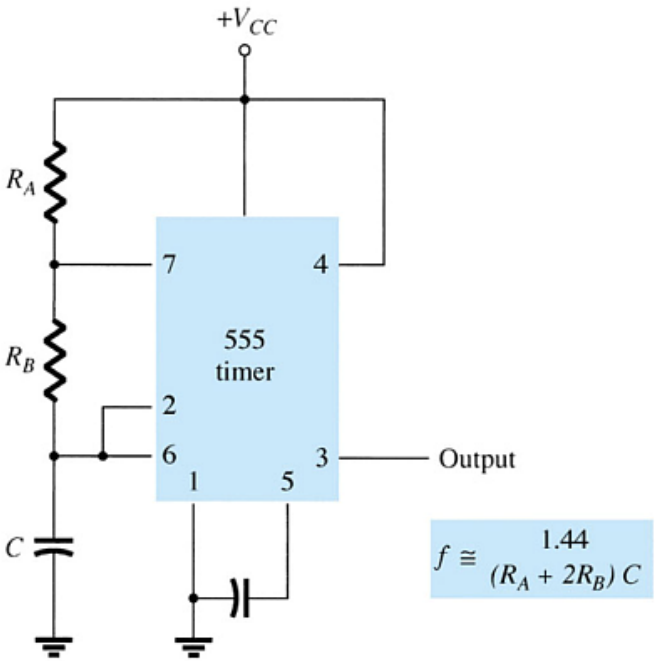
555 Timer Circuit

The 555 Timer is an example of a versatile Timer IC.

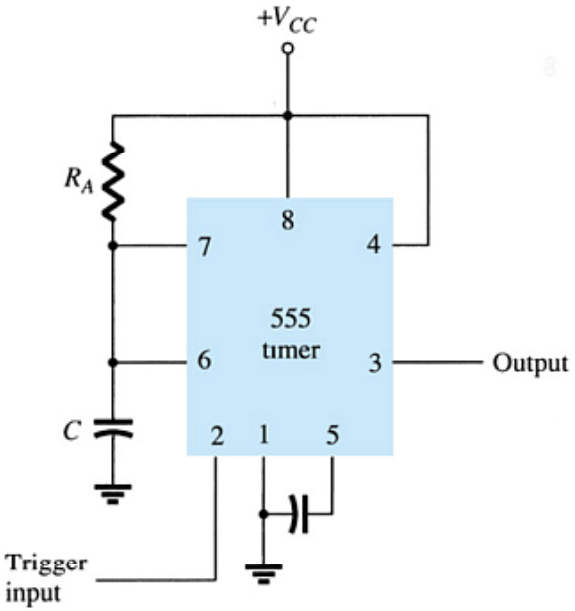
Astable Operation

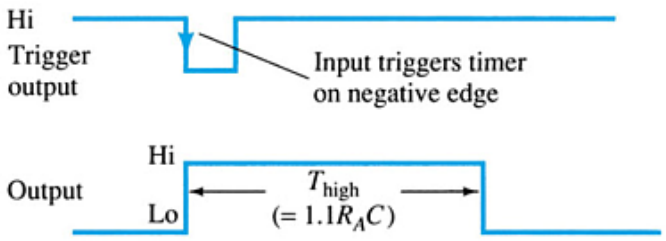
The timer output is a repetitive square wave. The output frequency can be calculated as shown here.





555 Timer Circuit

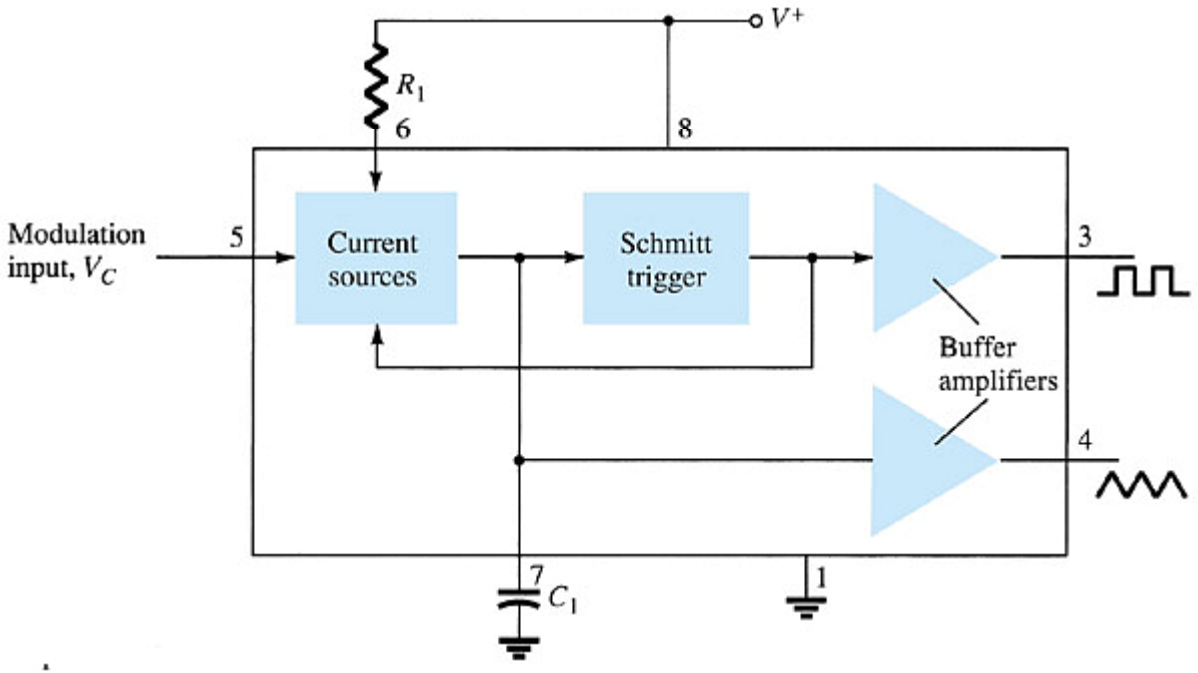




Monostable Operation

The timer output is a one shot pulse. When an input is received it triggers a one shot pulse. The time for which the output remains high can be calculated as shown.

Voltage-Controlled Oscillator

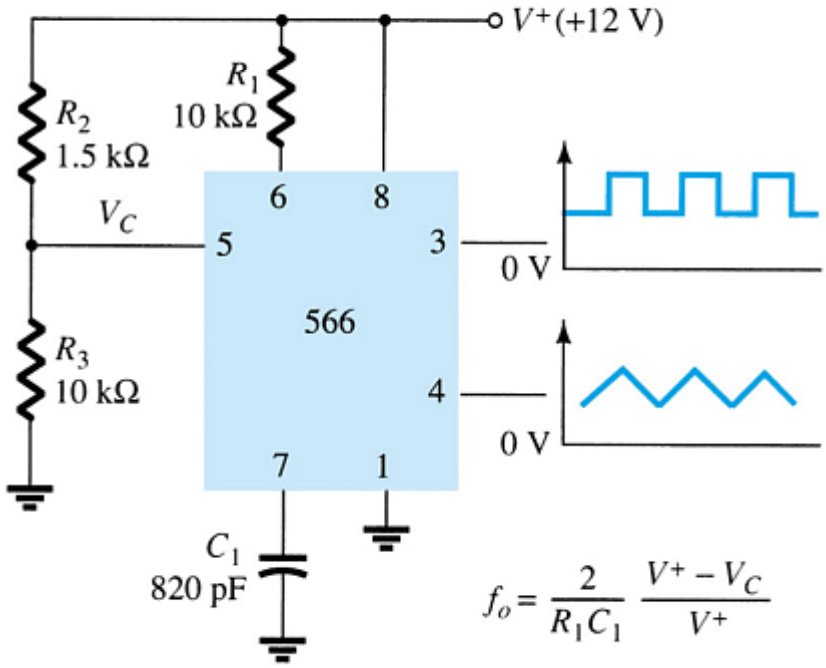


The oscillator output is a variable frequency square wave or triangular wave. The output frequency depends on the modulation input voltage (V_C).

566 Voltage-Controlled Oscillator

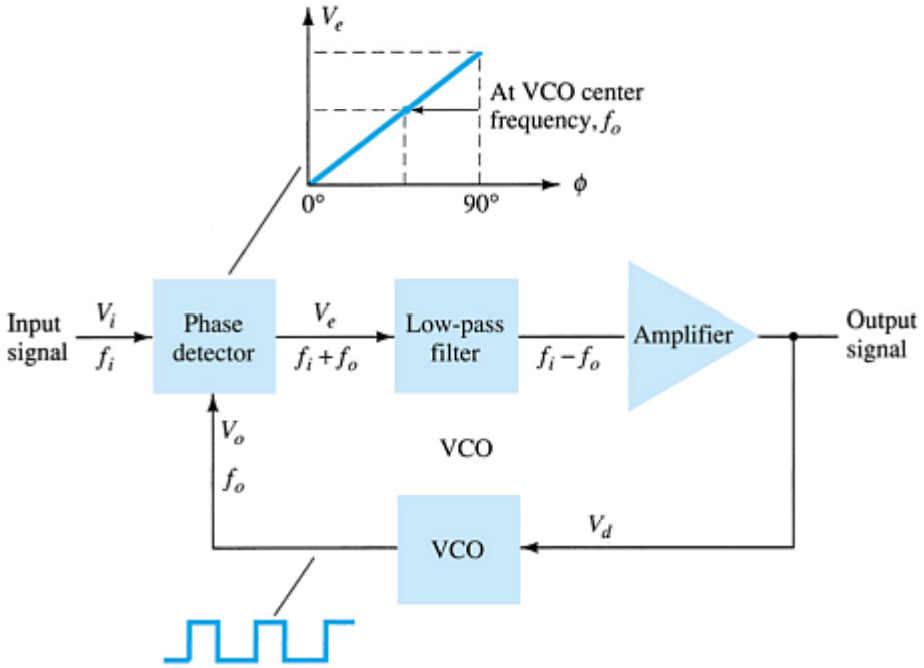
The output frequency can be calculated as shown in the graph.

Note that the formula also indicates other circuit parameters that affect the output frequency.



Phase-Locked Loop

The input signal is a frequency and the output signal is a voltage representing the difference in frequency between the input and the internal VCO.



Basic Operation of the Phase-Locked Loop

Three operating modes:

Lock

$$f_i = f_{VCO}$$

Tracking

$f_i \neq f_{VCO}$, but the f_{VCO} adjusts until $f_{VCO} = f_i$

Out-of-Lock

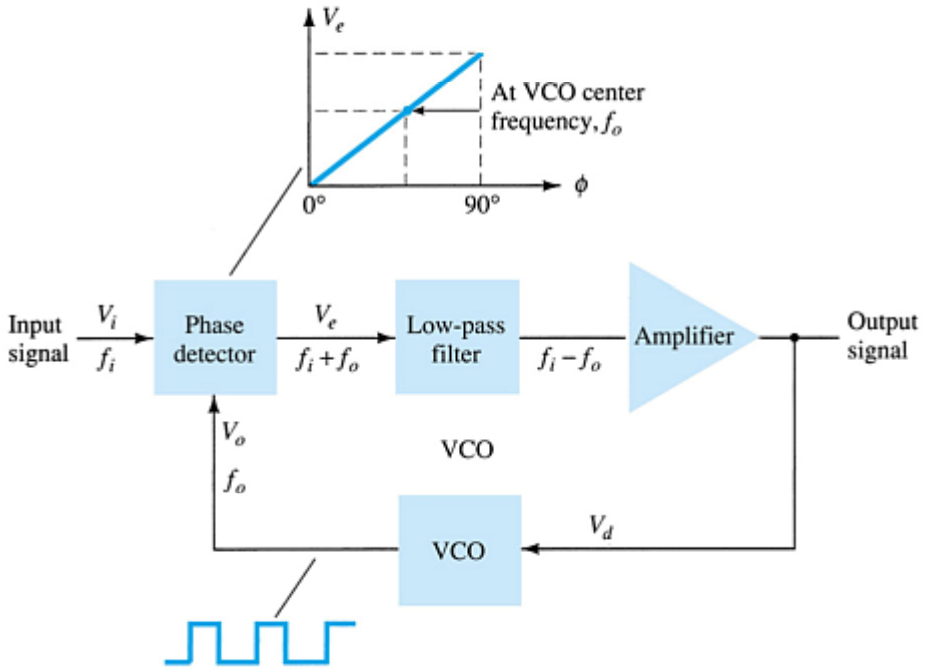
$f_i \neq f_{VCO}$, and they never will be the same

Phase-Locked Loop: Lock Mode

The input frequency and the internal VCO output frequency are applied to the phase comparator.

If they are the same, the phase comparator output voltage indicates no error.

This no-error voltage is filtered and amplified before it is made available to the output.



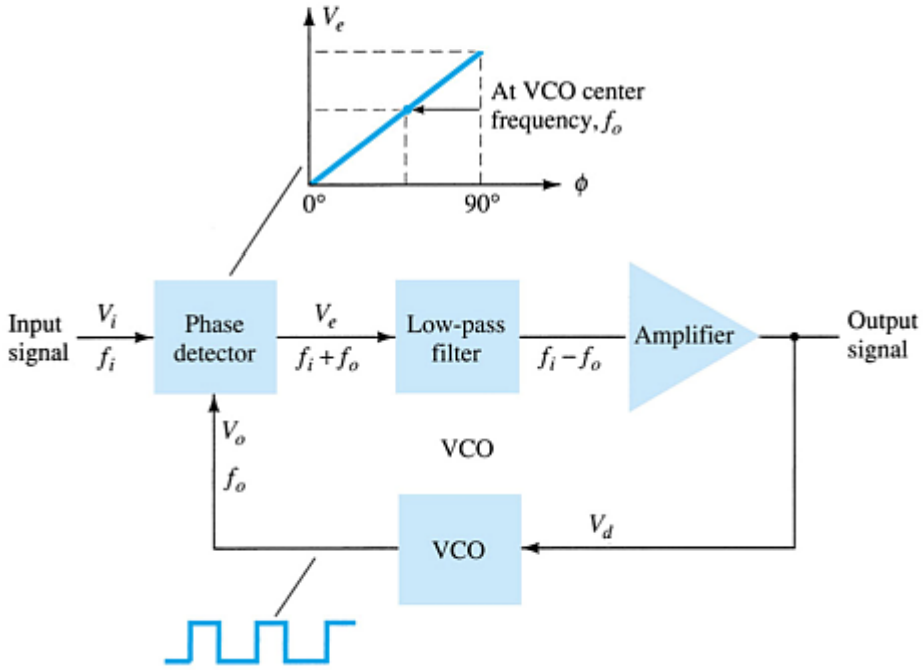
The no-error voltage is also applied to the internal VCO input to maintain the VCO's output frequency.

Phase-Locked Loop: Tracking Mode

If the input frequency *does not* equal the VCO frequency then the phase comparator outputs an error voltage.

This error voltage is filtered and amplified and made available to the output.

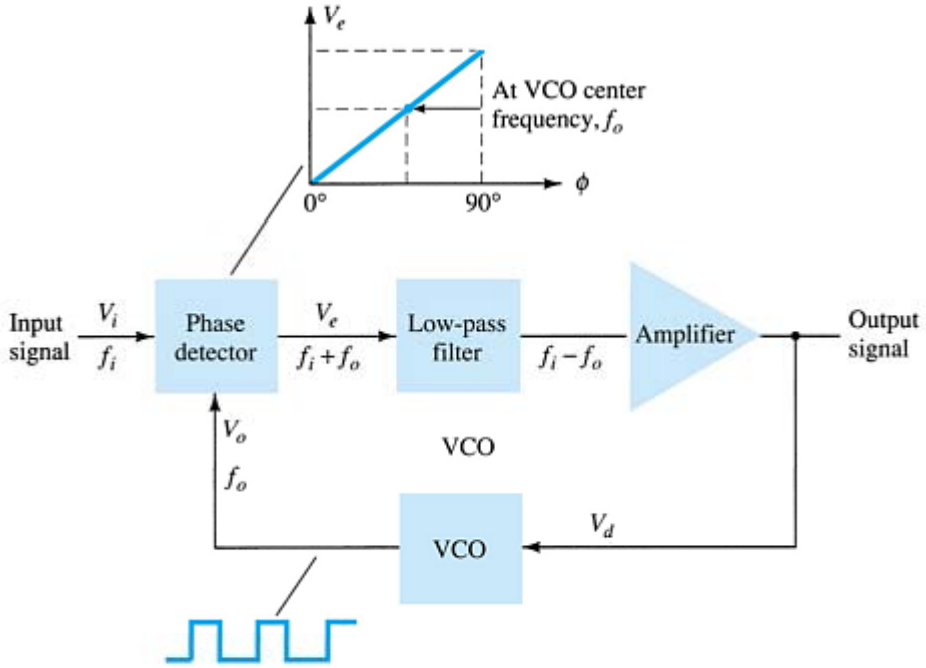
The error voltage is also applied to the VCO input. This causes the VCO to change output frequency.



This looping continues until the VCO has adjusted to the new input frequency and they are equal again.

Phase-Locked Loop: Out-of-Lock Mode

If the input frequency *does not* equal the VCO frequency and the resulting error voltage does not cause the VCO to catch up to the input frequency, then the system is out of lock. The VCO will never equal the input frequency.



Phase-Locked Loop: Frequency Ranges

Lock Range—The range of input frequencies for which the VCO will track.

Capture Range —A narrow range of frequencies into which the input frequency must fall before the VCO can track. If the input frequency falls out of the lock range it must first enter into the capture range.

Phase-Locked Loop

Applications:

- **FM demodulator**
- **Frequency Synthesizer**
- **FSK decoder**

Interface Circuitry

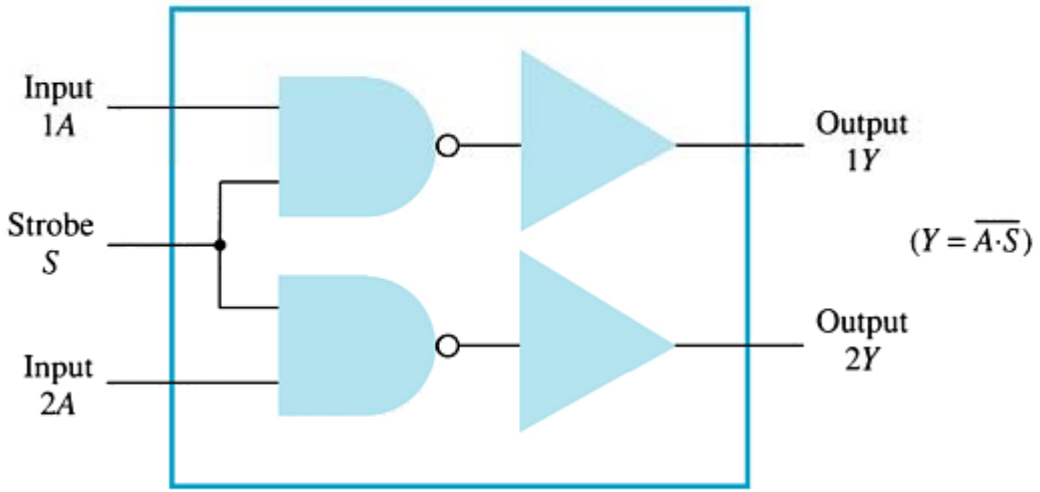
Interface circuitry:

- **Driving loads**
- **Producing output signals at proper voltage or current levels**
- **Impedance matching**
- **Strobing or timing signals**

Interface Circuitry: Dual Line Drivers

The input is TTL digital logic signal levels.

The output is capable of driving TTL or CMOS devise circuits.



RS-232-to-TTL Converter

The input is RS-232 electronic industry standard for serial communications.

The output will drive TTL circuitry.