

Cortex-M3 Architecture :

Introduction to the LPC1768 microcontroller

- Swarna Prabha Jena

Department of ECE

Index

- 1.1. Introduction: Embedded Systems+ Design of Digital Systems. The ARM Cortex-M3
- 1.2. LC1768: Block Diagram, Memory Map, Susses, Pinout
- 1.3. LPC1768 exceptions: Types and Vectors, NVIC, Enter+Exit, Priority, CM SIS functions.
- 1.4. LPC1768 system control modules: Clocking Features, RESET, FAULTs, SYSTICK, Power Management.

1.1. Embedded Systems

What is an Embedded System?

- Interacts with the environment
- Is divided into three stages: 1 INPUT+ 2 PROCESS + 3 OUTPUT
 - The processing is based on:
 - Combinational logic and sequential circuits
 - Microprocessors (μP) - Microcontrollers (μC)
 - Digital Signal Processor (DSP)
 - Programmable Logic Devices (PLDs)
 - Programmable Logic Controllers (PLCs)
 - In general, they are real-time reactive systems:
 - They react to external events and keep continuous interaction
 - They are continuously running
 - Their work is subjected to external time constraints
 - They do concurrently several tasks

1.1. Design of Digital Systems

A microcontroller (μC) is a chip **that includes in a single chip** all elements needed in a digital system

- the processor (μP , CPU)
- different types and amounts of memory and
- various input/output interfaces and peripherals
- All of them interconnected by uni/bidirectional busses

Therefore:

- Achieving more integration and lower price
- Lower time to market when implementing a project

1.1. The ARM Cortex-M3

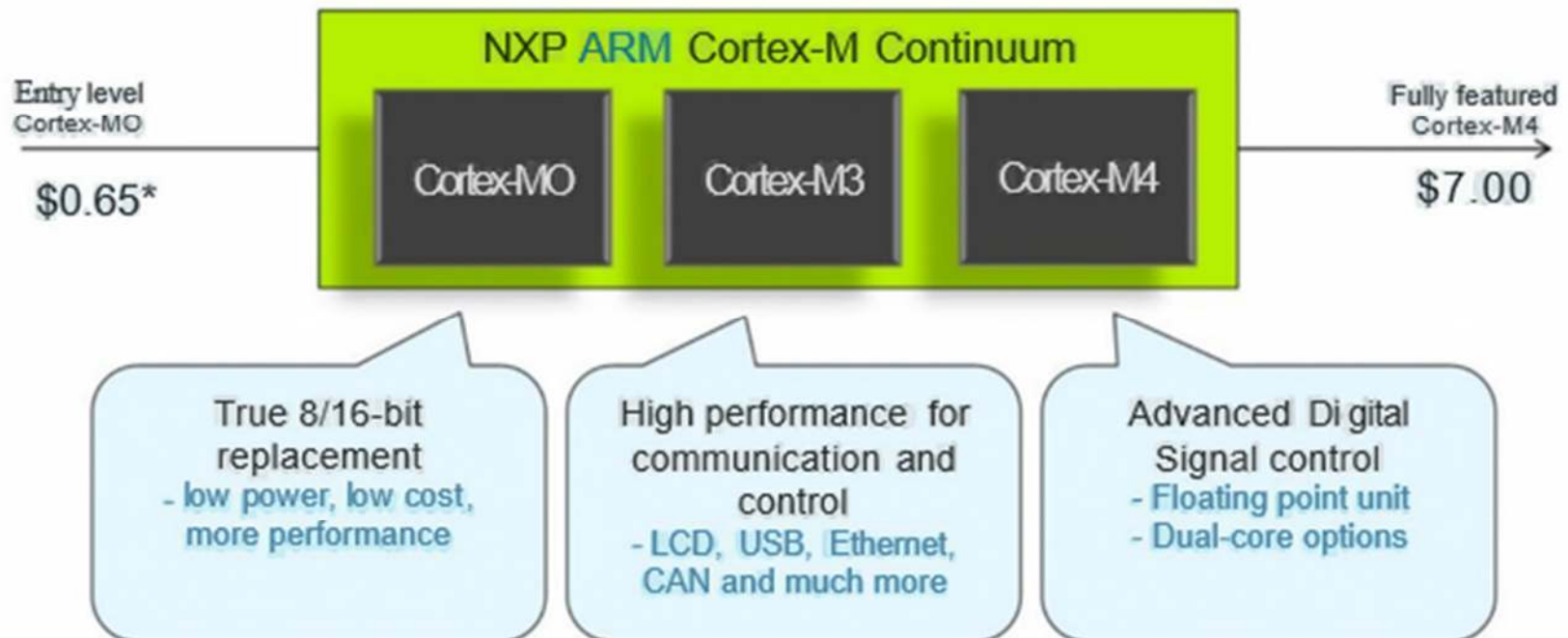
ARM is a:

- RISC μ P
- 17/18 32 bits visible registers in its programmer's model (37 total)
- a Cach~ Memory (upon version)
- Von Neuman architecture (ARM7)
- Harvard architecture (ARM9 and forward)

The Cortex-M3 C builds on the success of the ARM7

- Nonmaskable interrupts for critical tasks
- Deterministic nested vector exceptions
- Atomic bit manipulation
- Optional Memory Protection Unit (MPU)

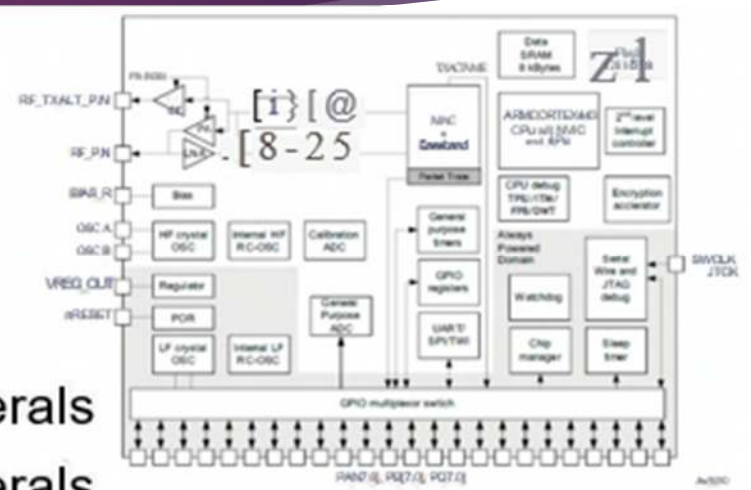
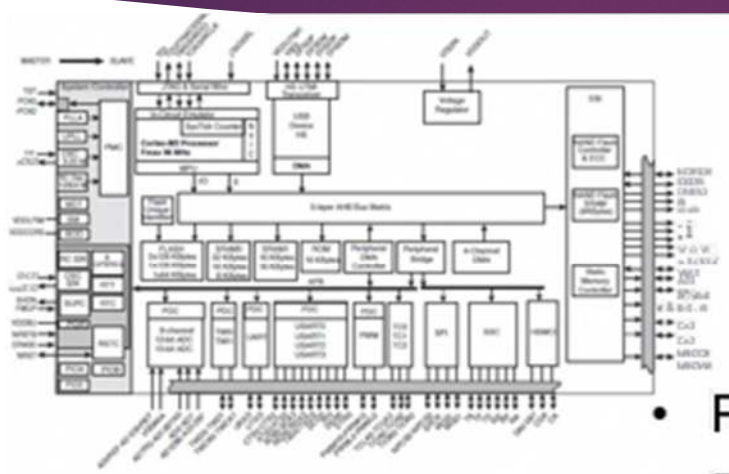
1.1. ARM Cortex Advanced Processors



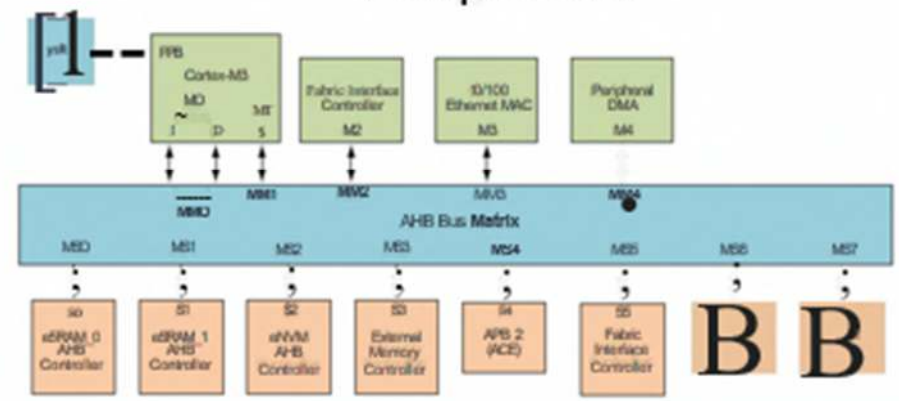
1.1. Cortex-M3: Manufacturers



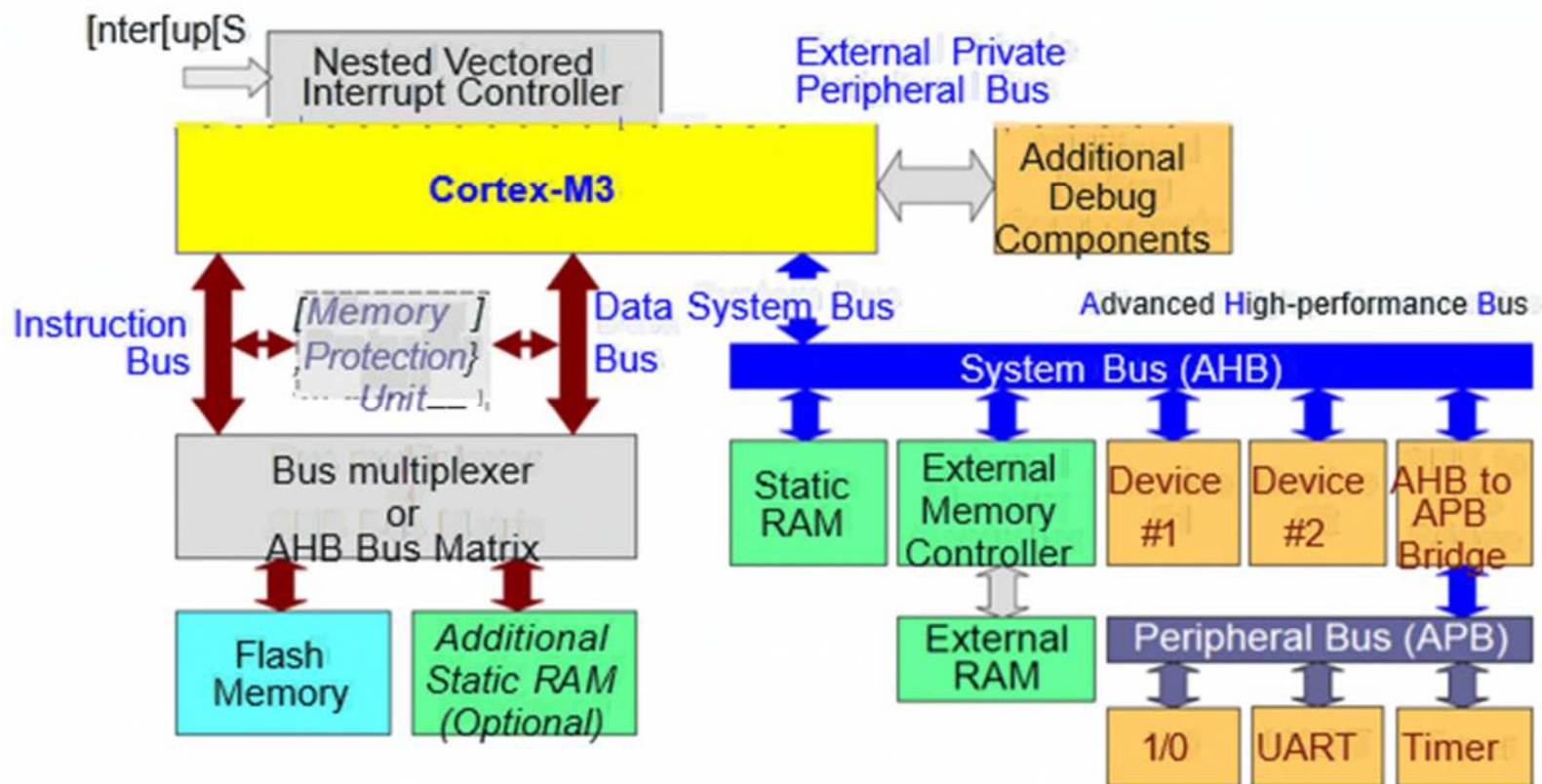
1.1. Manufacturers that incorporate Cortex-M3: Differences?



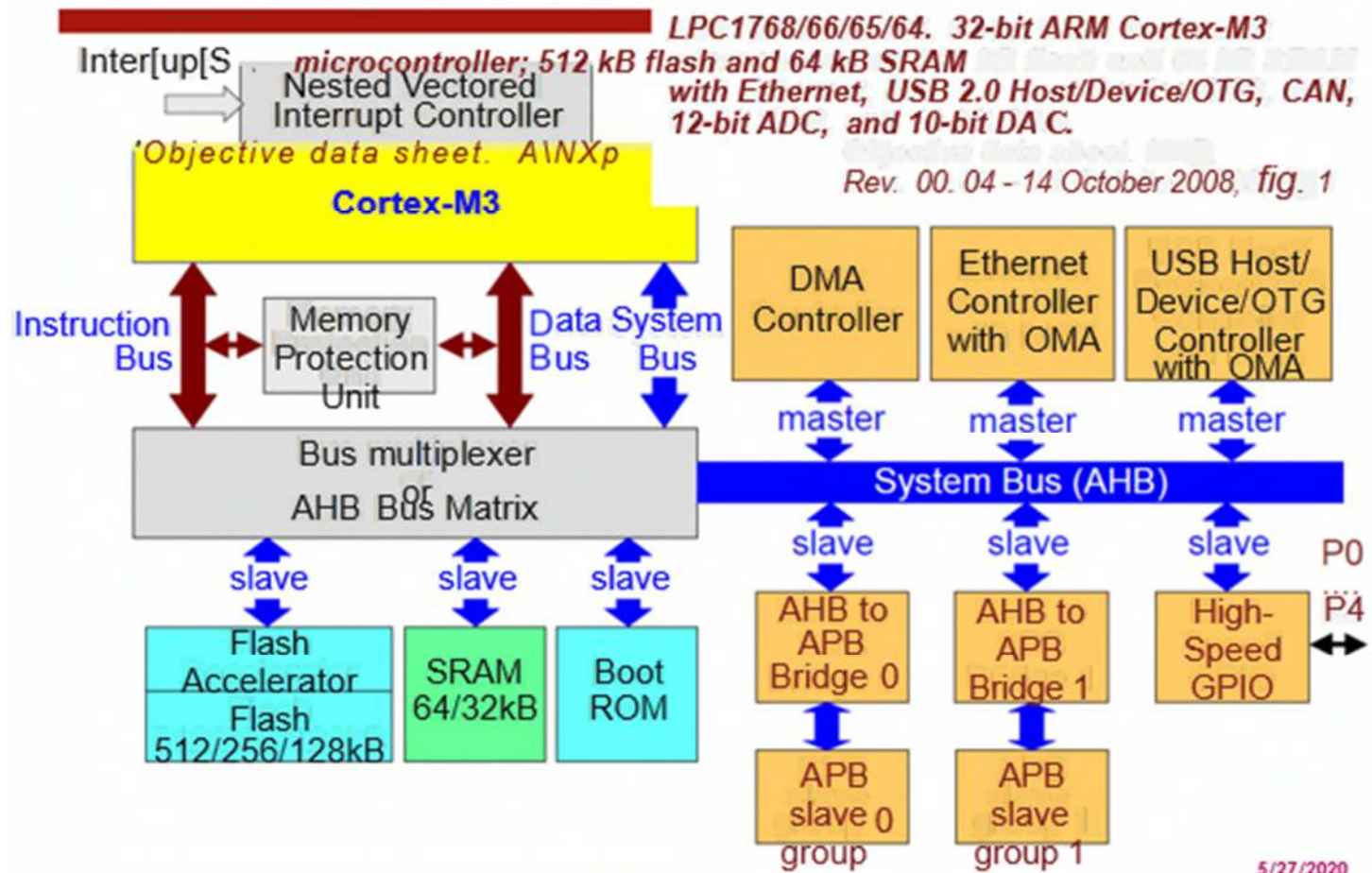
- Peripherals
- Peripherals
- Peripherals



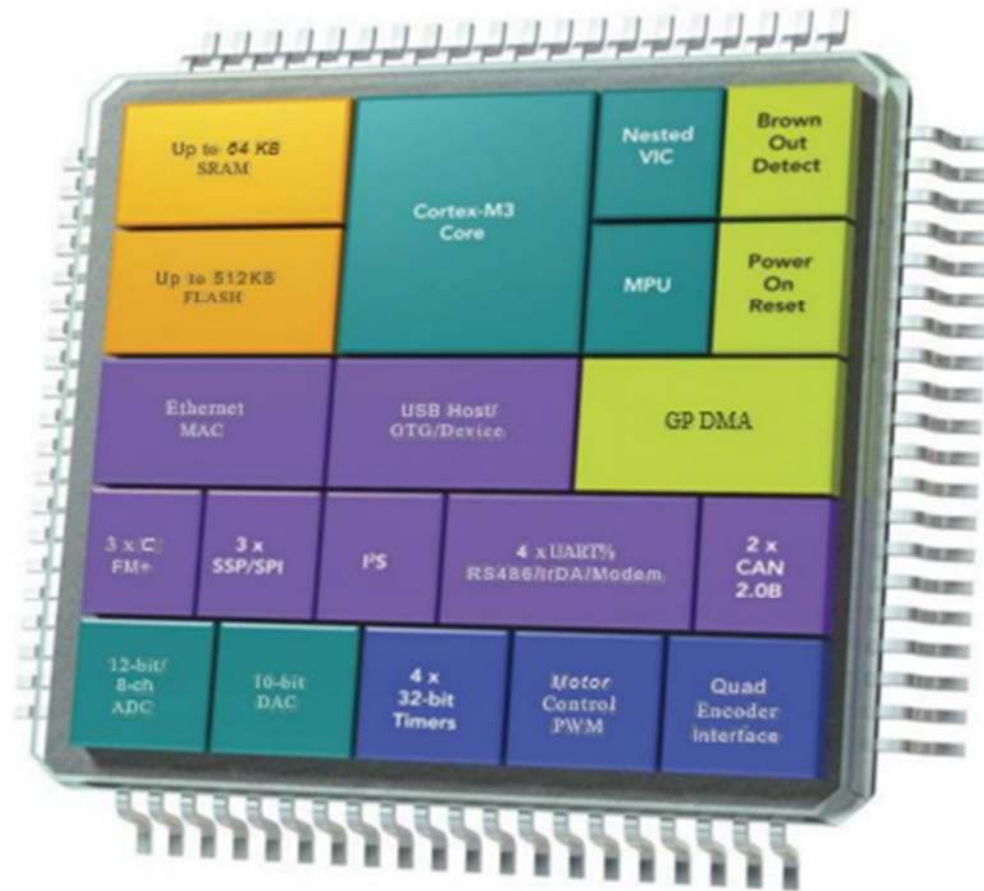
1.2. Cortex-M3: Busses



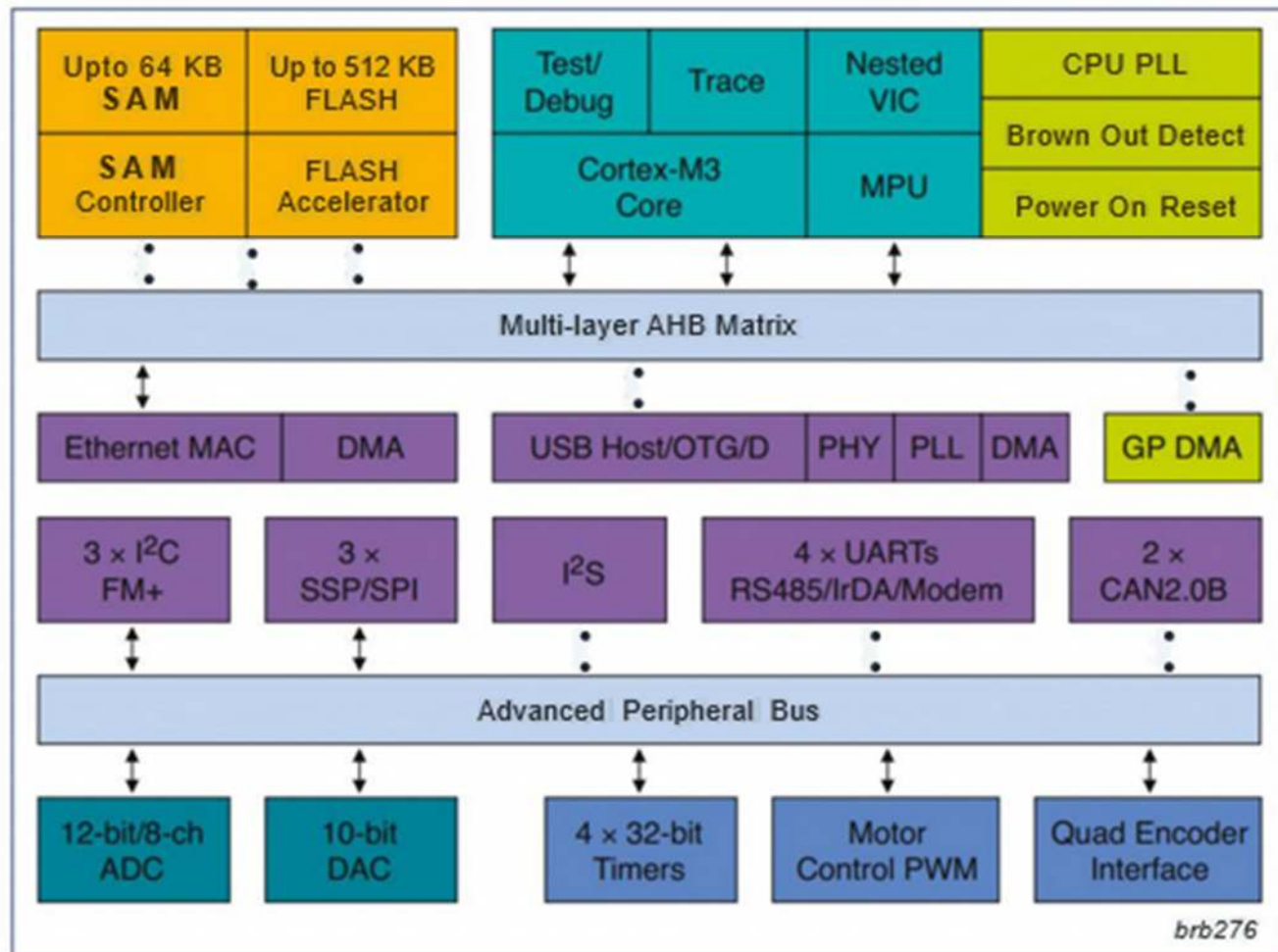
1.2. LPC17xx: Busses



1.2. LPC17xx: Block Diagram



1.2. LPC17xx: Block Diagram



1.2. LPC17xx: Memory

13

D On-chip Flash

- Maximum 512 KB.
- Zero wait-state performance with Flash Accelerator.

□ On-Chip SRAM

- Maximum 64 KB:
 - 32 KB SRAM - accessible by the CPU and DMA controller on a higher speed bus.
 - Two additional 16 KB SRAM - separate slave port on the AHB multilayer matrix.
 - Allows CPU and DMA accesses to be spread over 3 separate RAMs that can be accessed simultaneously.

D On-Chip ROM

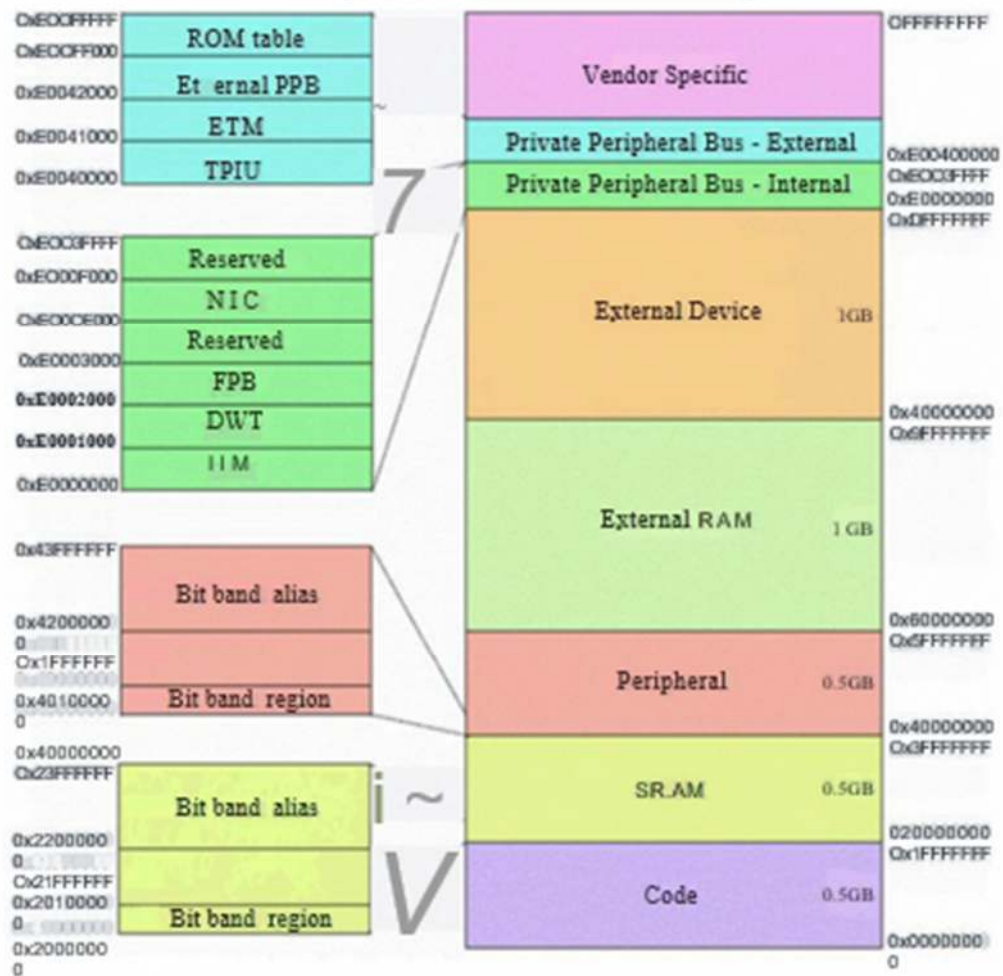
- 8 KB ROM.
- Flash program/erase APIs.
- Used for booting - not customer accessible.

5/27/2020

1.2. LPC17xx: Family

Part Number	Max Clock (MHz)	E I R E			USB	E I I E E I					I/O Pins	Package
LPC1769	120	512	64	Y	Device/Host/OTG	2	Y	8	Y	3	70	LQFP100
LPC1768	100	512	64	Y	Device/Host/OTG	2	Y	8	Y	3	70	LOFP100
LPC1767	100	512	64	Y	None	0	Y	8	Y	3	70	LOFP100
LPC1766	100	256	64	Y	Device/Host/OTG	2	Y	8	Y	3	70	LQFP100
LPC1765	100	256	64	N	Device/Host/OTG	2	Y	8	Y	3	70	LOFP100
LPC1764	100	128	32	Y	Device	2	N	8	N	3	70	LQFP100
LPC1759	120	512	64	N	Device/Host/OTG	2	Y	6	Y	2	52	LOFP80
LPC1758	100	512	64	Y	Device/Host/OTG	2	Y	6	Y	2	52	LOFP80
LPC1756	100	256	32	N	Device/Host/OTG	2	Y	6	Y	2	52	LOFP80
LPC1754	100	128	32	N	Device/Host/OTG	1	N	6	Y	2	52	LQFP80
LPC1752	100	64	16	N	Device	1	N	6	N	2	52	LQFP80
LPC1751	100	32	8	N	Device	1	N	6	N	2	52	LOFP80

1.2. Cortex-M3: Memory Map

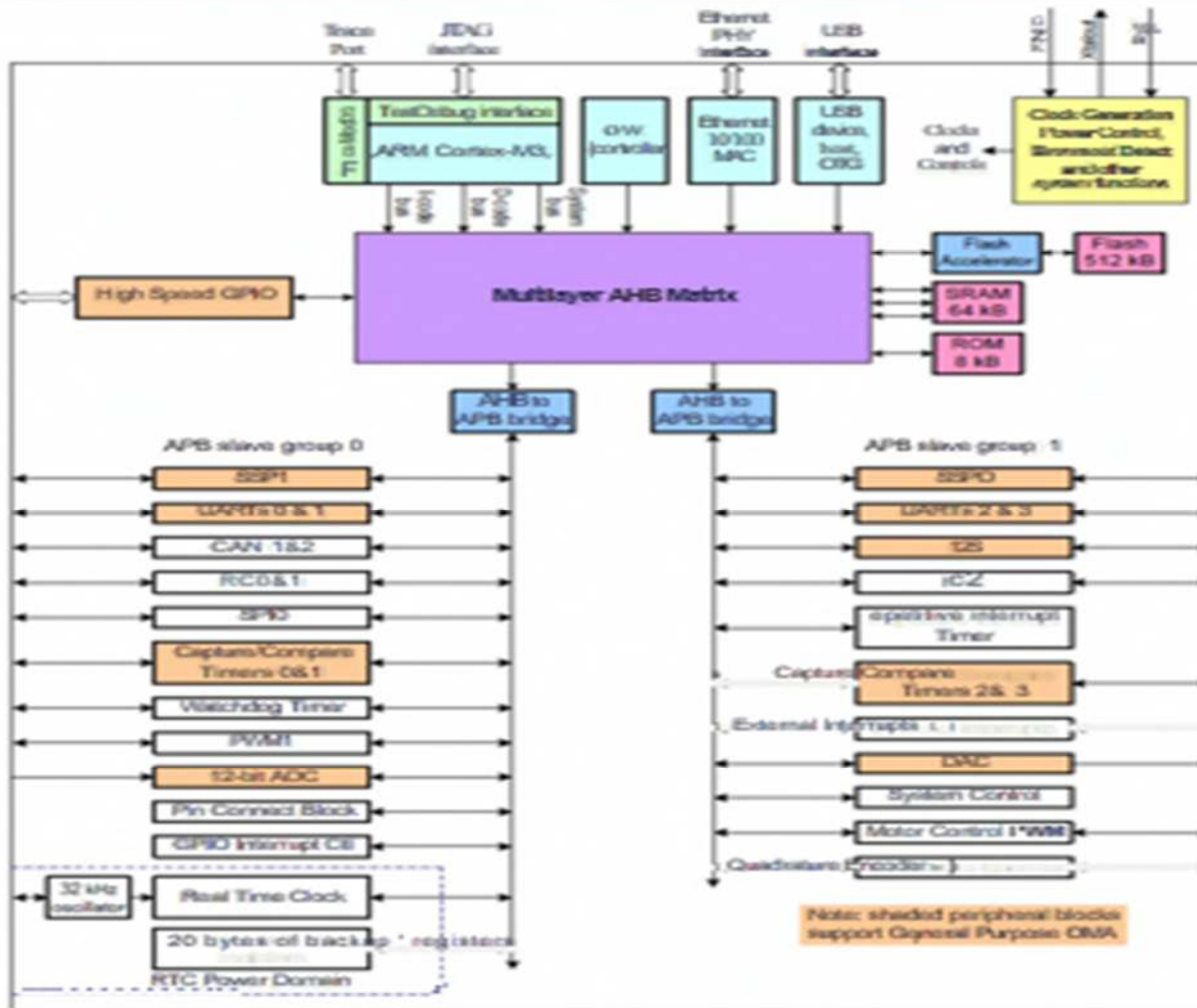


1.2. LPC17xx: Memory Map

Table 3. LPC17xx memory usage and details

Address range	General Use	Address range details and description	
0x0000 0000 to 0X1FFF FFFF	On-chip non-volatile memory	0x0000 0000 - 0x0007 FFFF	For devices with 512 kB of flash memory.
		0x0000 0000 - 0x0003 FFFF	For devices with 256 kB of flash memory.
		0x0000 0000 - 0x0001 FFFF	For devices with 128 kB of flash memory.
		0x0000 0000 - 0x0000 FFFF	For devices with 64 kB of flash memory.
		0x0000 0000 - 0x0000 7FFF	For devices with 32 kB of flash memory.
	On-chip SRAM	0x1000 0000 - 0X1000 7FFF	For devices with 32 kB of local SRAM.
		0x1000 0000 - 0X1000 3FFF	For devices with 16 kB of local SRAM.
		0x1000 0000 - 0X1000 1FFF	For devices with 8 kB of local SRAM.
	Boot ROM	0X1FFF 0000 - 0X1FFF 1FFF	8 kB Boot ROM with flash services.
0x2000 0000 to 0X3FFF FFFF	On-chip SRAM (typically used for peripheral data)	0x2007 C000 - 0X2007 FFFF	AHB SRAM - bank 0 (16 kB), present on devices with 32 kB or 64 kB of total SRAM.
		0x2008 0000 - 02008 3FFF	AHB SRAM - bank 1 (16 kB), present on devices with 64 kB of total SRAM.
	GPIO	0x2009 C000 - 0X2009 FFFF	GPIO.
0x4000 0000 to 0x5FFF FFFF	APB Peripherals	0x4000 0000 - 0x4007 FFFF	APB0 Peripherals, up to 32 peripheral blocks, 16B each.
		0x4008 0000 - 0X400F FFFF	APB1 Peripherals, up to 32 peripheral blocks, 16 kB each.
	AHB peripherals	0x5000 0000 - 0X51F FFFF	DMA Controller, Ethernet interface, and USB interface.
0xE000 0000 to 0xE00F FFFF	Cortex-M3 Private Peripheral Bus	0xE000 0000 - 0XE00F FFFF	Cortex-M3 related functions, includes the NVIC and System TickTimer.

1.2. LPC1768: Bus structure



1.2. LPC1768: Bus structure (Multilayer AHB Matrix)

